FEB2 "Slice" Testboard Update

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NEVIS LABORATORIES
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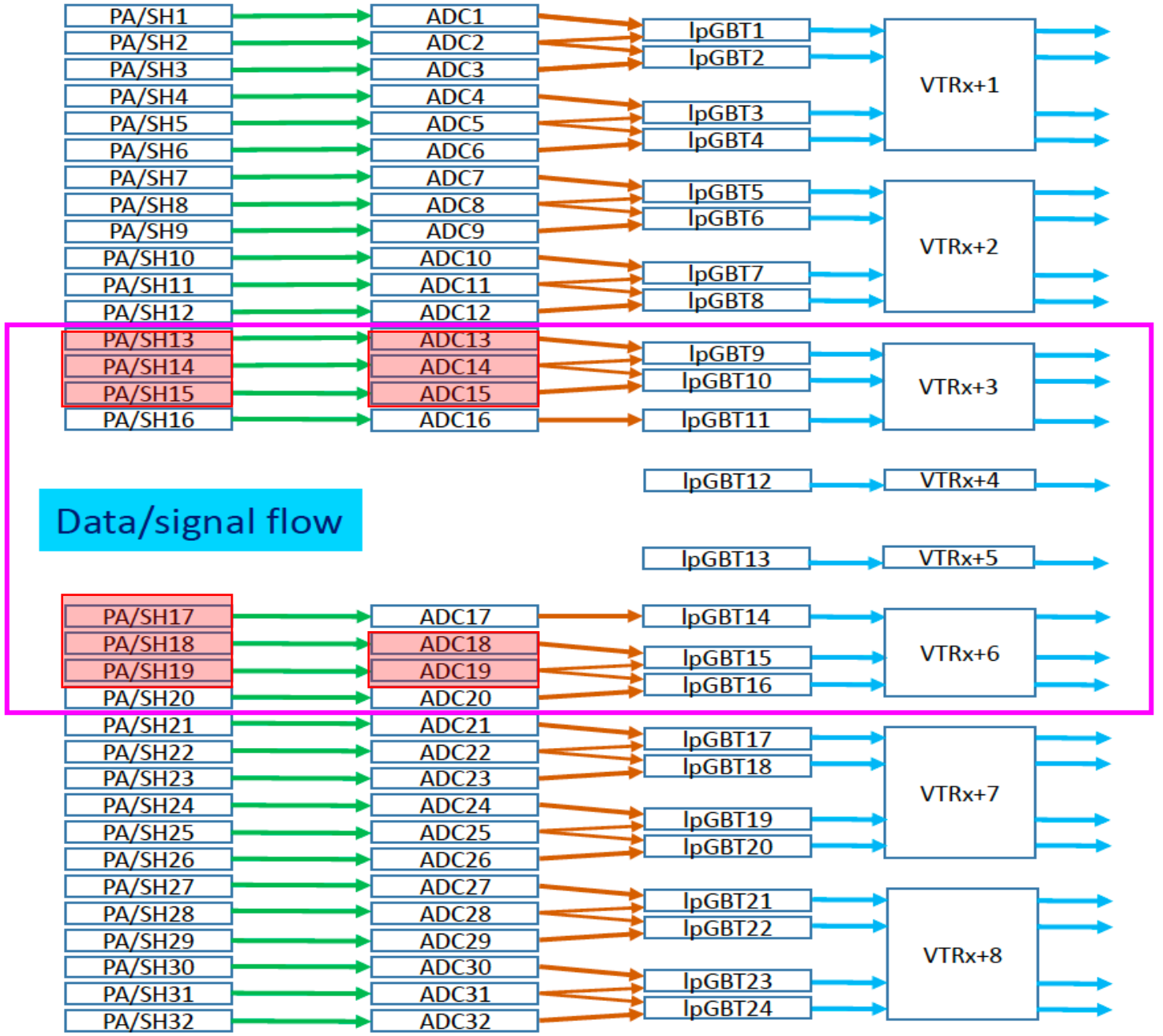
ATLAS EXPERIMENT

Overview

- Analog Testboard (2019)
  - 2 (LAUROC1 PA/S + COLUTAv2 ADC) + lpGBT
  - Verified full readout chain PA/S + ADC + optical data links
- Slice Testboard (2020)
  - 8 (LAUROC2/ALFE1B PA/S + COLUTAv3 ADC + lpGBT) chips, 32 LAr channels available
  - Aim to demonstrate multichannel performance, bi-directional control links
  - v1.0 of the board (being tested at Nevis now) is only partially assembled to reduce the number of custom ASICs needed, since there are a limited number available
- Full FEB2 Prototype (2021-2022)
  - All 128 channels

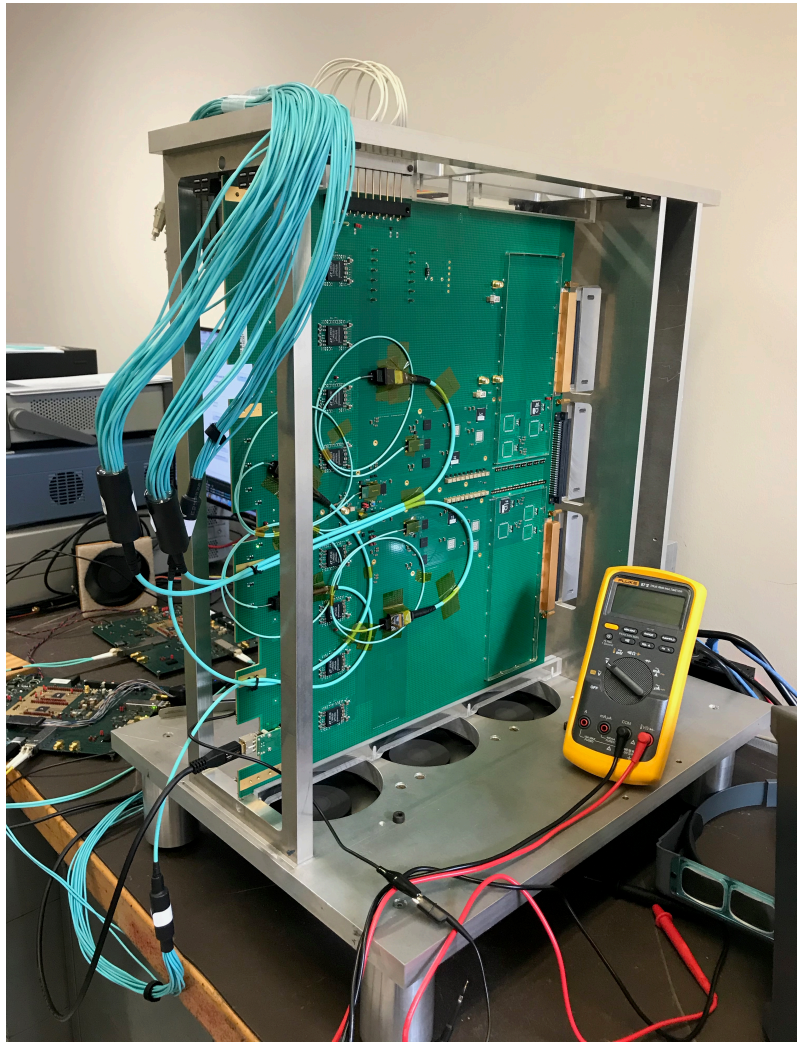
Review: FEB2 Data/Signal Flow



Chip not included on partially assembled boards

Summary of October LAr Week Presentation

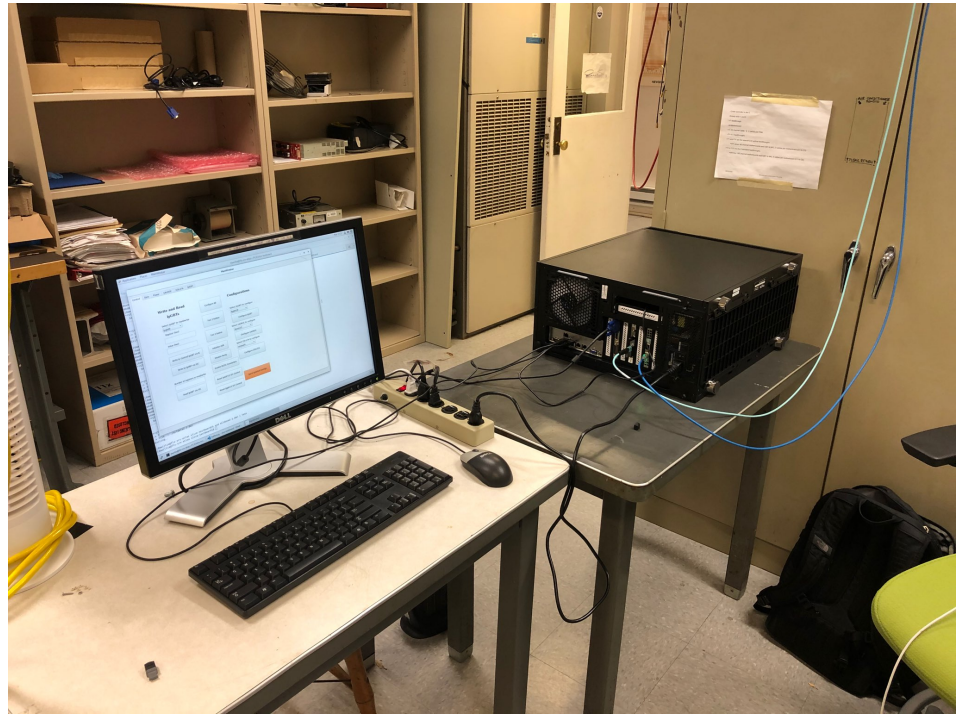
- ✓Resolved lpGBT M2 bus issues and burned e-fuses on both control lpGBTs
- ✓Developed and demonstrated control set up using FPGA on Analog Testboard, and external USB
- ✓Configured and read back all ASIC types (control lpGBTs, data lpGBTs, ADCs, PA/Ss)
- ✓Read correct test pattern data from data lpGBTs and ADCs via the optical uplink
- ✓Pulsed PA/S and read back via the optical uplink



October LAr Week Presentation here

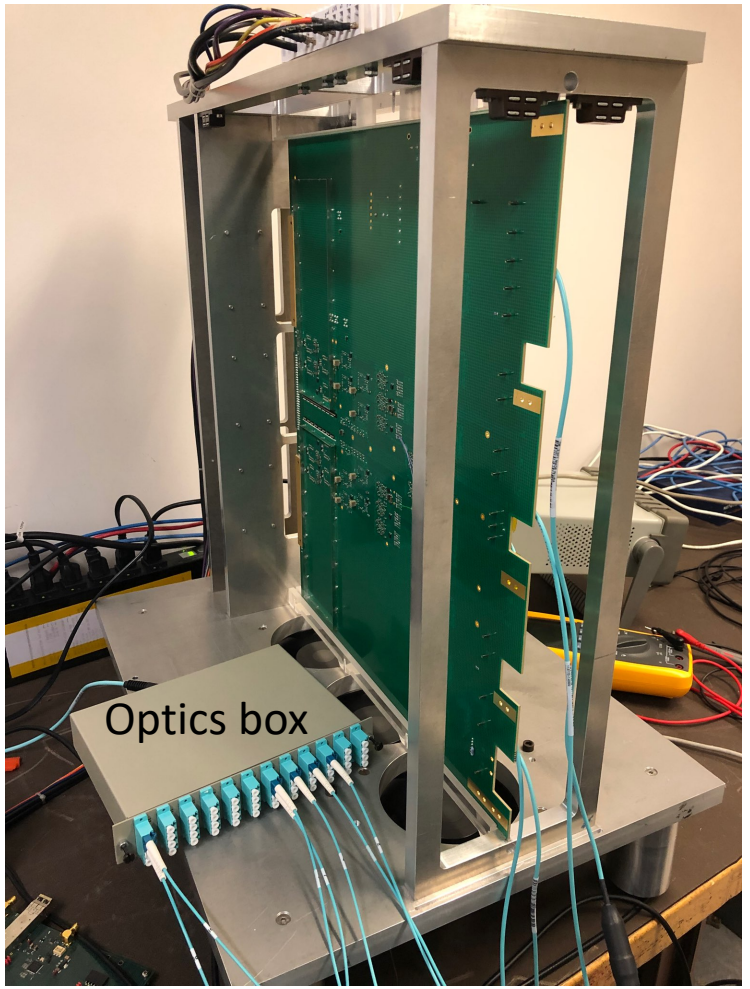
Migration to FLX

- During previous LAr week, FLX card arrived at Nevis
  - Compatibility issues with the first server delivered to Nevis
  - We were able to make progress by temporarily borrowing a server from the Nevis DUNE group
  - Upgraded ATLAS server arrived at Nevis Dec 2nd, server is now fully functional
- FLX card allows full control of both sides of the board



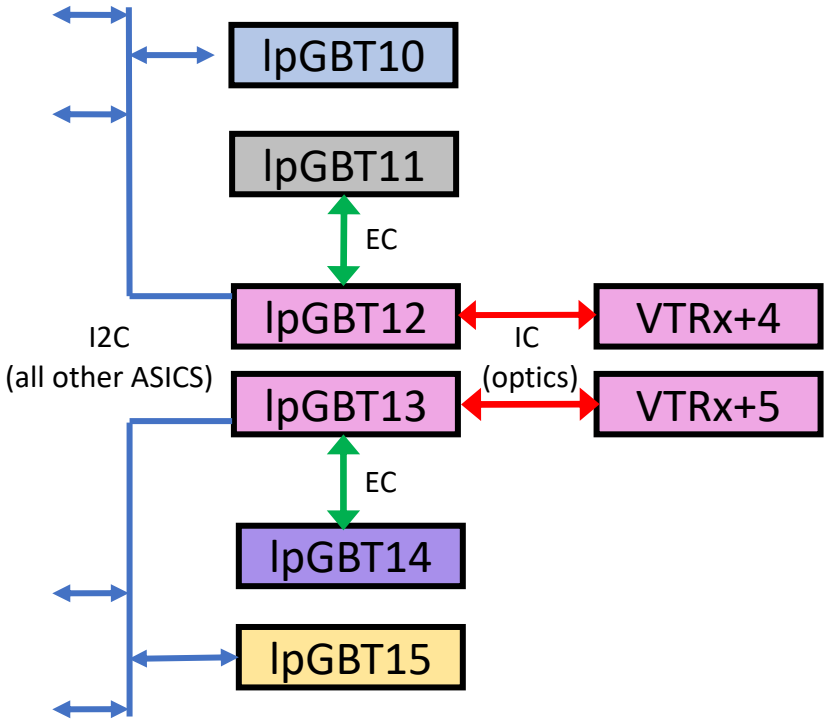
Benefits of FLX

- With FLX we can talk to both lpGBT12 and lpGBT13 at once
  - With the Analog Testboard/ USB we could only talk to one or the other
- With FLX we can read out all 6 data fibers at once
  - With the Analog Testboard we could only read one



Configuring the board with FLX

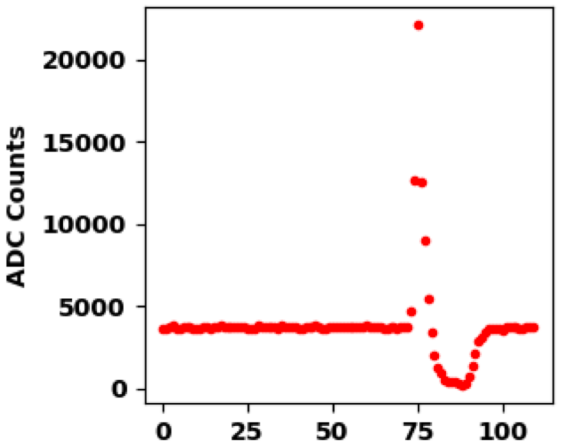
- We successfully replicated all tests performed with the USB/ Analog Testboard control
  - IC communication (write and readback) from FLX to control lpGBTs 12 and 13
  - I2C communication (write and readback) with all secondary ASICs via the control lpGBTs
- Established EC control links for lpgbt 11 & 14
  - E-fuses blown so that 11 & 14 always come up in EC mode
- We were able to migrate our software control suite to FLX with relatively few issues



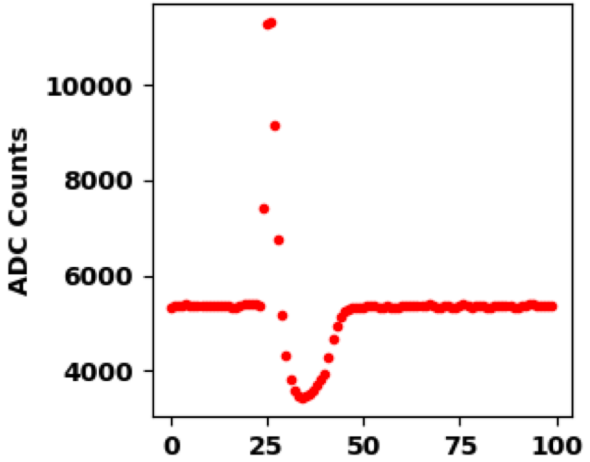
Reading Data with FLX

- Demonstrated data read out from all available ADCs (ADC20, ADC17, ADC16) at once
  - Found the correct clock settings for each ADC/ data lpGBT pair
  - Confirmed that we see the correct serializer data from the ADCs
- Finished validation of the v1.0 Slice Testboard design by reading data through all available channels
  - Observed physics pulse through LAUROC20 & LAUROC16
  - Few minor PCB design changes prior to submission of v1.1 PCB fabrication

Pulse through LAUROC20 (from Oct)



Pulse through LAUROC16



Timeline (updates since Oct LAr Week Presentation)

- ✓ Oct 5 - FLX card received at Nevis
- ✓ Oct 12 - Start to use FLX to control and read out entire Slice Testboard
- ✓ Nov 16 - Complete validation of Slice Testboard design, and proceed with fabrication of (slightly modified) PCBs with PCB vendor 2

- ➢ ~~Dec 7~~ Dec 24 - Receive new PCBs and submit for assembly
- ➢ ~~Jan 4~~ Jan 25 - Begin testing of new fully assembled boards
- ➢ ~~Feb 15~~ Mar 8 - Ready to deliver first board to collaborators

Next Steps

- We plan to build 5 new fully assembled v1.1 Slice Testboards, since we have just enough lpGBT chips for 5 boards (no additional lpGBT chips are available)
- LAL/Omega currently has sufficient LAUROC chips to fully assemble the first 2 boards only (8 chips each)
  - They will package more chips for the other 3 boards, but for administrative reasons they cannot place this order until January
- We will start by assembling the first 2 boards so we can begin testing and send 1-2 boards to our collaborators as soon as possible
- We will assemble and test the 3 additional boards once we receive sufficient LAUROC chips

Conclusions

- We have fully validated the functionality of the Slice Testboard design and fabrication of new PCBs is underway
- We have begun performance evaluation of the board and will continue in the coming weeks
- We have demonstrated full control of the board using a FLX card, as well as communication via the external USB and an Analog Testboard
- We are on track to send boards to our collaborators in early 2021