COLUTA and FEB2 Updates

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on behalf of the COLUTA and FEB2 teams

ATLAS HL-LHC Upgrade Project LAr ADC & FEB2
March 8, 2023

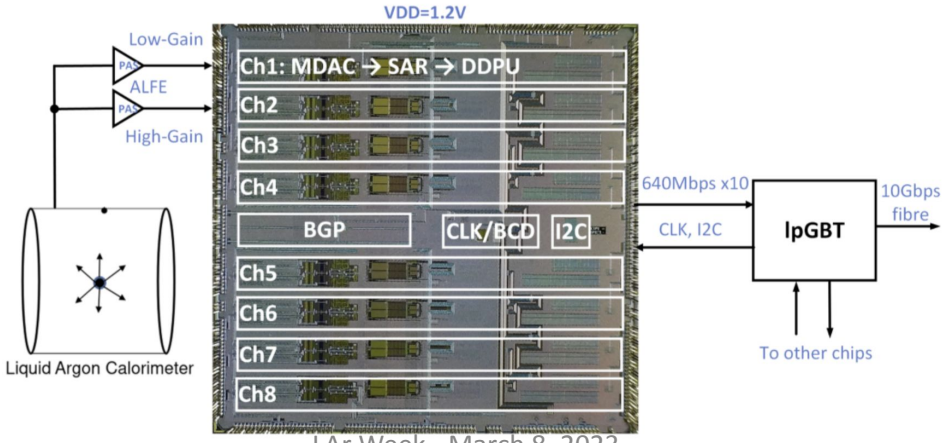
Outline

- COLUTA Update
- FEB2 Update
- Conclusions

COLUTA Update

COLUTA ADC

- custom designed ADC for radiation hardness-> 4th version (COLUTAV4 / CV4)
  - end goal: ~80k chips
  - digitize input from PA/S
  - MDAC (multiplying DAC) with 3 bits in front of SAR (successive approximation) with 12 bits
  - 8 identical Channels of MDAC & SAR & DDPU (digital data processing unit)
    - 15 bits of Dynamic Range (MDAC chosen over DRE ADC after COLUTAV3) with an additional overflow bit -> 16 bits
  - on CV4 testboard,
    - ch 1 - 4: (ch 1 &4: transformer ch 2: commercial amplifier; ch3 commercial DAC)
    - ch 5 - 8: connected to high / low gain pairs from ALFE2

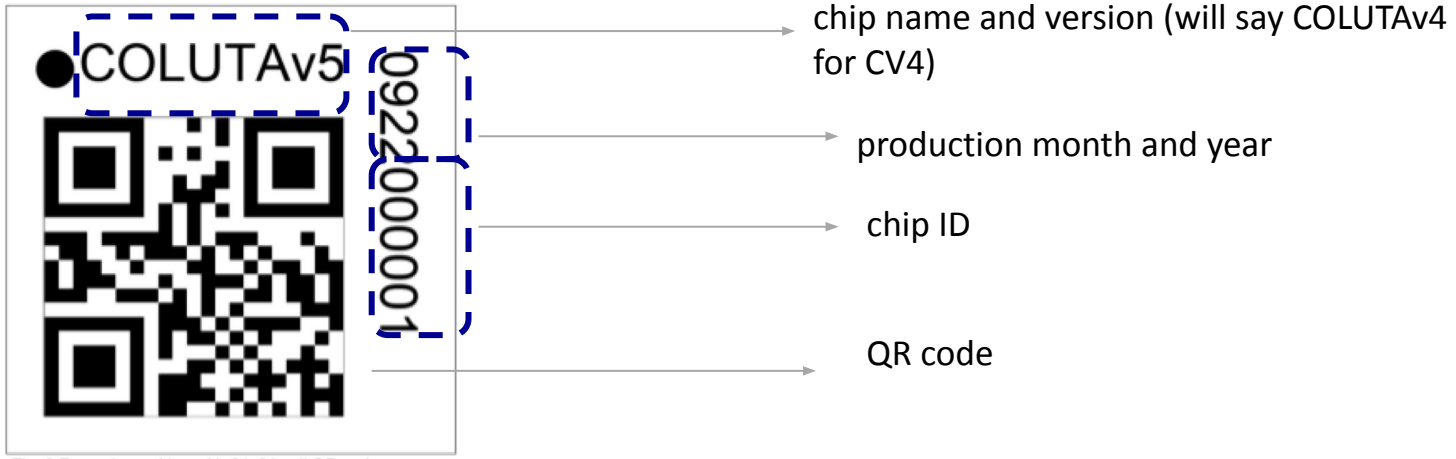


ADC Final Design Review

- link to the FDR, which was held on Oct. 7, 2022
  - https://indico.cern.ch/event/1191836/
- review was passed with recommendations and received the green light to submit COLUTAV4 as the preproduction (and then later production) version
  - "The team plans to use the existing prototype design as a pre-production design for an engineering run submission. The review panel supports this proposal."
- since COLUTAV4 meets all the specifications, so no need for CV5 (original plan)
- Pre-production order submitted, masks produced and 5 wafers were received at CERN Feb. 22nd, 2023. Wafers being shipped to JCET for packaging

BGA Packaging

- changing packaging from QFN to BGA as part of preparation for production
- progress/plan:
  - additional CV4 dice (400) ordered from MPW run. Chips arrived at CERN in January and were shipped to JCET (packager)
  - JCET has the CV4 chip and packaging is in progress. However, no firm date for delivery yet.
  - recall, purchase order made in May 2022 for JCET who has done the design to package CV4 in the BGAs (same vendor as for ALFE2)
  - Ready to start testing BGA packaged CV4 chips as soon as we receive them from packager.
- BGA (ball-out grid array) Package should include:
  - unique QR code (can be read by automated cameras during QC testing) & human readable information

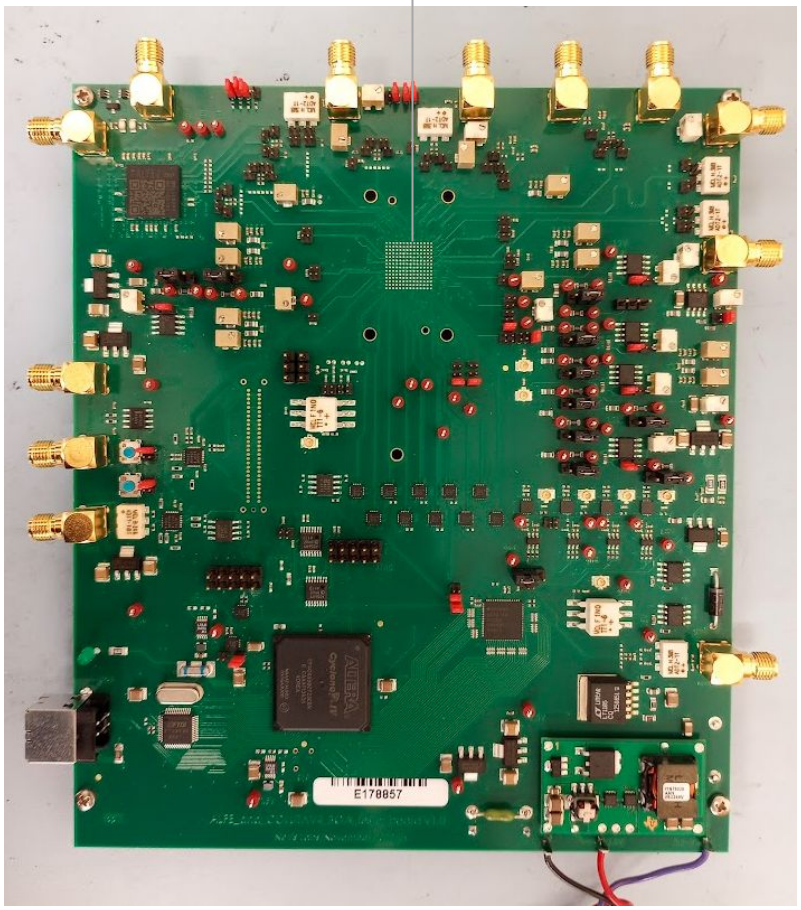


CV4 BGA testboard

- new version of COLUTAV4 testboard
  - designed and produced implementing both COLUTAV4s and ALFE2s in BGA packages
  - 3 produced and they are working; also tested to the extent possible before receiving CV4s where computer can talk to FPGA and FPGA can control the ALFE

- next steps:
  - 1. validate that CV4s in BGA packages give the similar performance as the ones in QFN packages (results shown in FDR)
  - 2. validate the integration of CV4s and ALFE2s both in BGA packages
  - 3. select some CV4 BGA packaged chips to use for the first FEB2 prototype boards

where BGA packaged CV4 would be placed

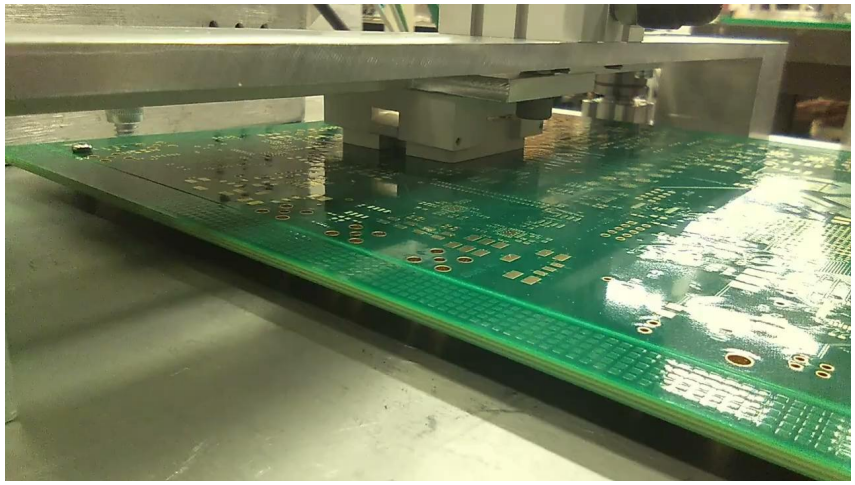


Quality Control (QC) Testing

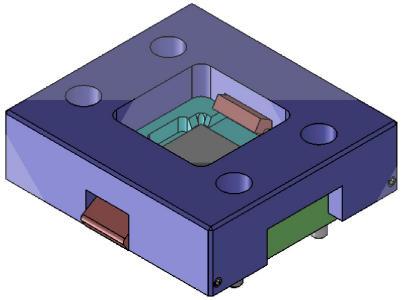
- motivation:
  - need to select high quality COLUTAV4 chips for them to be assembled onto FEB2 boards
- plan for future:
  - ~80k chips to be tested by the UT Austin (50%) and Paris-Saclay (50%);
  - Saclay's QC test development be presented later this meeting
- UT Austin team is using designs created by Lund University SAMPA team
- automation using robotic arms (Yamaha YK500XGL) controlled by PC
  - motivated by a) faster testing for a large number of chips (~40k) b) ability to retest
  - includes transfer of chip between tray and socket using vacuum gripper, verifying chip's location, recording and reading QR codes of the chips by a camera attached to the robotic arm

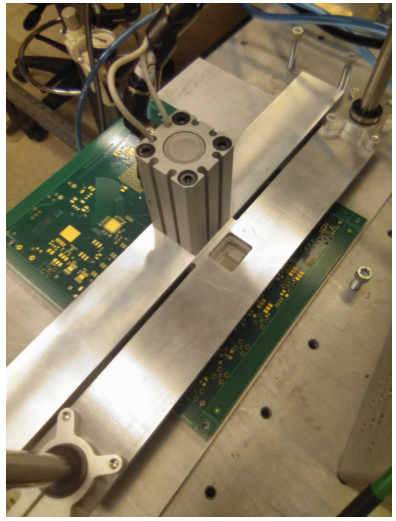
CV4 Mass QC Testing

- ADC testing criteria (in progress):
  - basic functions: estimated to take < 1 min
    - chip power on, communication signals received (e.g. clock signal & chip control), initializing configurations
  - performance & precision: estimated ~ 1 min
    - physics performance e.g. dynamic range, energy & timing resolutions
    - precision e.g. ENOB, INL & DNL



- progress/plan:
  - December: chose VAI socket (socket type/manufacturing company); ordered 4 sockets; camera integrated to the robotic test stand
  - Current:
    - 3 sockets in Nevis and 1 in UT Austin
    - tested and verified camera's ability to read of the sample QR codes (on the BGA packaging slide) and improved the light condition on the test stand
    - design of socket actuator complete
    - integrating the socket actuator and robotic arm into a system
  - future: program, using the GUI, the integrated system to open the socket and place a dummy BGA chip inside

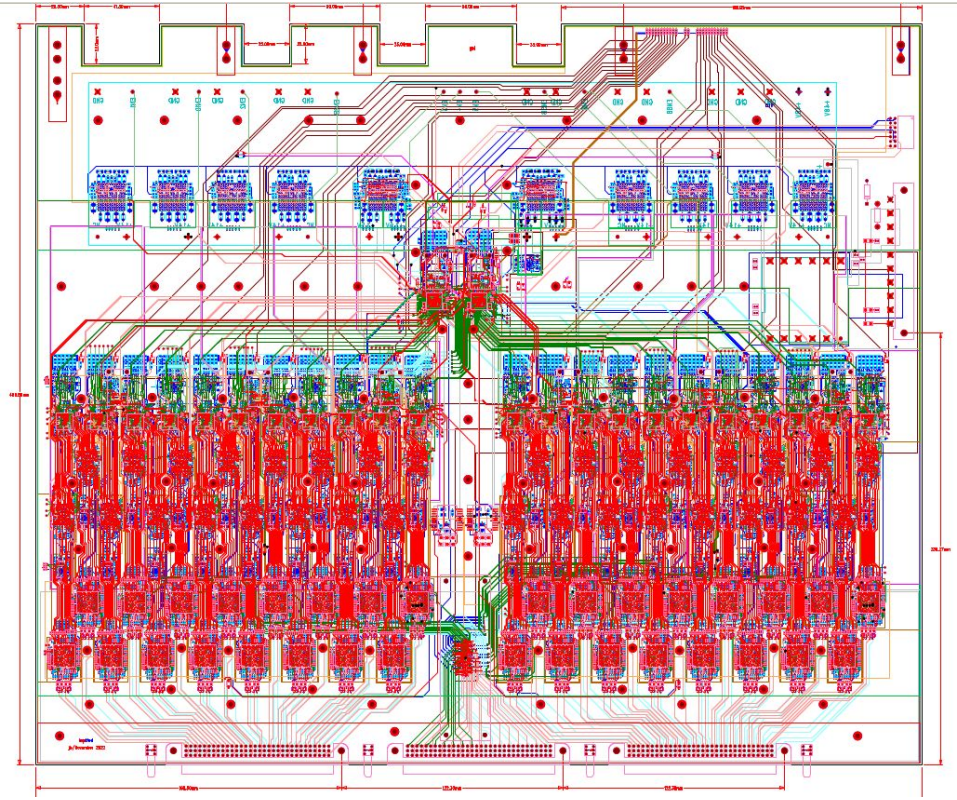




FEB2 Update

FEB2 Prototype Design Status

- at the FEB2 PDR (held on Dec. 9, 2022), received an approval to fabricate v1 of FEB2 prototype
  - https://indico.cern.ch/event/1203223/
- v1 of FEB2 Prototype
  - recall that it was decided to make v1 of FEB2 Prototype with power mezzanines, to allow us to proceed with fabrication and testing now while rad-tol powering scheme is being finalized
  - v1 FEB2 Prototype design now complete (shown on the right)
  - after recent discussion, design was modified to allow test of option where Control lpGBTs (12/13) are powered with 1.2V directly from DC-DC convertor (ie. without using CMS LDO)
- twiki pages
  - FEB2 Prototype design information being gathered: https://twiki.nevis.columbia.edu/twiki/bin/view/ATLAS/FEB2Prototype
  - detailed instructions on how to configure the FEB2 Prototype: https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/FEB2Prototype/sliceBoardFeb2Protoboard_i2cConfiguration.pdf



FEB2 Prototype - Next Steps

- orders placed:
  - to fabricate 5 bare PCBs for v1 FEB2 Prototypes
  - to first partially assemble 2 boards, with goal of testing and debugging all the (very many) changes since the Slice Testboard

- steps for assembly
  - due to limited availability, in first step will populate only 8 sets of ALFE2 + COLUTAv4 + associated CMS LDO, providing 32-channel readout (as on the Slice Testboard); this "saves" 24 of each of these components per board
  - all 24 lpGBT chips will be populated, to allow testing of full control architecture, including new features such as EC (external control) link implementation with all lpGBT chips present. (One half of board can also be configured to test the EC link with half of the lpGBTs connected.)

FEB2 Prototype - Next Steps (continued)

- steps for assembly (continued)
  - have received at Nevis all custom components needed for first boards, including 100 CMS LDOs, 120 lpGBT, 100 VTRx+, 20 ALFE2 in BGA. Only thing still missing is CV4 in BGA, for which we will have to wait until they are available and tested
  - once partially assembled v1 boards tested, if no need for significant PCB change is identified, could assemble another 2 boards, this time with all 128 channels fully populated (instead of 32)
  - once v1 testing is complete, complete v2 (and hopefully final) FEB2 Prototype design with final powering scheme, with goal to be able to start delivering the first of 14 boards needed for the Front End Crates System Test at BNL during the fall

Closing Remarks

- COLUTA:
  - expect to have CV4s in BGA packages delivered soon
  - have the testboards ready for testing
  - in parallel, preparing robotic test for mass QC testing

- FEB2:
  - v1 FEB2 prototype is in the PCB fabrication step
  - assembly of the first 2 v1 (partially assembled) boards will be ready to proceed once CV4s in BGA packages are available

BACKUP

Summary of ADC Final Design Review

- https://indico.cern.ch/event/1191836/
- performance measurements that met / exceeded specifications (backup slides) through tests with ADC and ADC integrated with PA/S (ALFE2) → confirmed by the review panel

- additional review panel feedback:
  - comments:
    - ADC power consumption specification increase from <100 mW/ch to 143mW/ch is acceptable given that the water cooling capacity allows it
    - PSRR (power supply rejection rate) is less than 60dB (specification) at <1MHz but it has no significant effect on energy/timing resolution
    - only 18 COLUTAv4 chips have been tested so limited statistics
  - recommendations:
    - performance:
      - investigate harmonics observed in ENOB measurement
      - see how COLUTAv4 logic and conversion cycles react to the temporary distortions in the lpGBT input clock to simulate real-life clock distortion during LHC operations
    - packing and testing
      - check the time it takes to test one chip
      - test ALFE by packaging BGA with the COLUTAv4 and looking at its functionality

      conclusion: “The team plans to use the existing prototype design as a pre-production design for an engineering run submission. The review panel supports this proposal.”

ADC Specifications

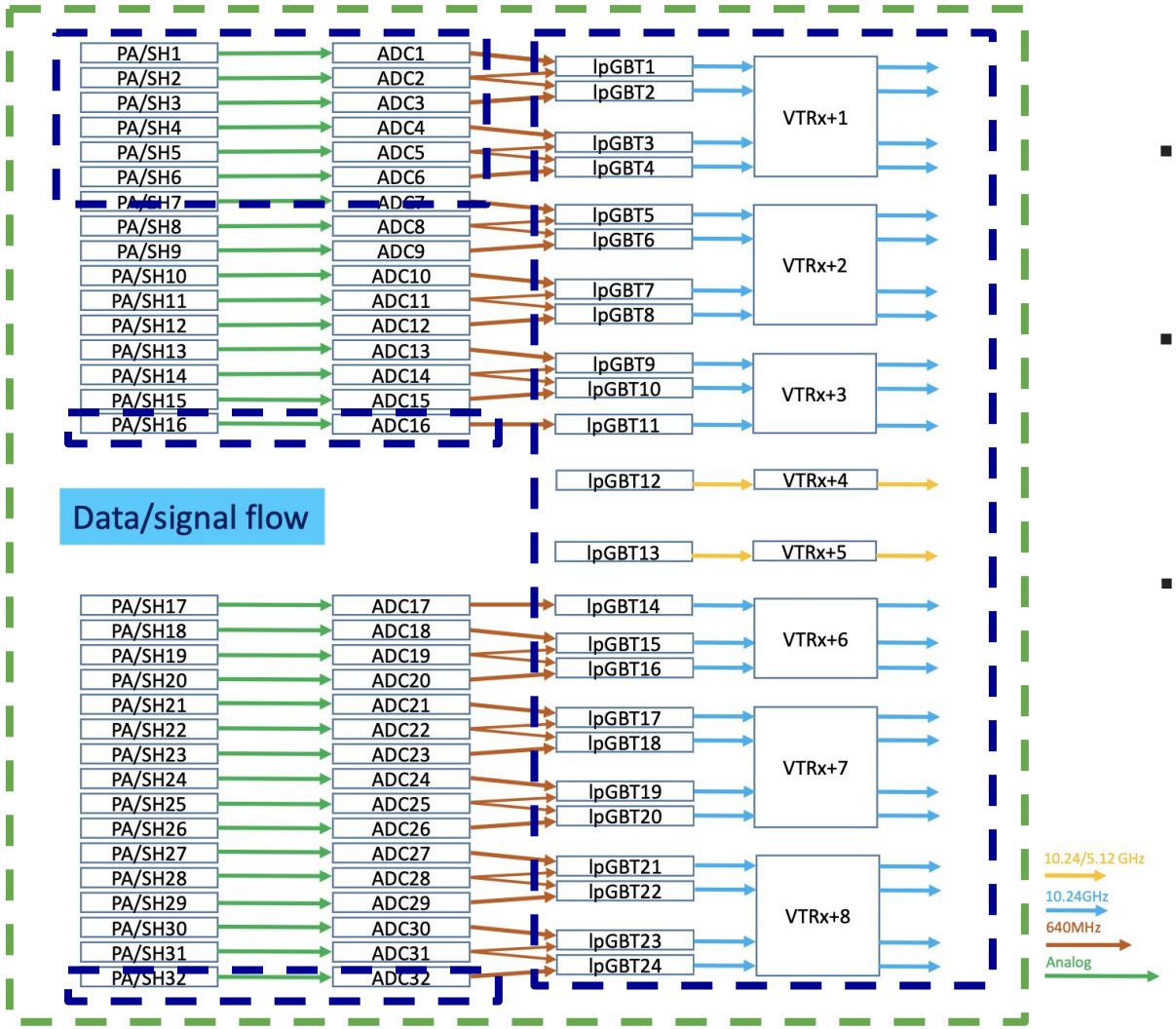
Table 1: Performance specifications for the ADC.

Parameters	Specification
Channels/chip	8 preferred, 4 minimum ✔
Sampling Frequency	40 MSPS ✔
Dynamic Range	14 bits ✔
Precision	11 ENOB at 8 MHz ✔ MDAC + SAR sine ENOB 11.8 @ 8 MHz
Power	<100 mW/channel X Mean 143 mW/channel – acceptable given updated FEB2 spec
Input	2 V differential ✔
Output	E-link interface operating at 640 Mbps ✔
Operating temperature	From 10 to 50° C (optimal 20° C) ✔
Temperature range not requiring a new calibration	5° C ✔
Calibration duration	less than a few minutes ✔
Calibration frequency	at most every few hours ✔

- Fraction of coherent noise between channels should be less than 0.2 LSB RMS. ✔ From Slice Testboard: coherent noise ~0.15 LSB RMS
- Power Supply Rejection Ratio (PSRR) should be 60 dB or higher. ✔ Somewhat lower at lower f, however no significant degradation of measurement resolution observed
- Integral Non Linearity (INL) must be better than 0.1% up to 60% of the total dynamic range (i.e. from ADC code 3000 to 9800), and better than 1% at 80% of total dynamic range (from ADC code 3000 to 13000). The INL can be up to a few (4) percent at 100% of the dynamic range (code 3000 to 16383). A somewhat degraded linearity from ADC code 0 to 1000 is acceptable, since this corresponds to the undershoot of high amplitude signals. The undershoot is not used for energy/time extraction. ✔ INL < 0.02 % across dynamic range
- Differential non-linearity (DNL) should be less than ±1.0 12-bit LSB and there should be no missing codes. ✔ ✔ DNL < ±1.0 LSB, no missing codes
- The gain error should be correctable with calibration. The calibration frequency should be at most once/day. The gain and offset stabilities should be better than 0.1% over the temperature range. TO DO THIS WEEK?
- Cross-talk between channels should be less than 0.5%. Cross-talk is expressed as the amplitude (peak-to-peak) on the neighboring channel at the peak of the pulsed channel, divided by the peak-to-peak amplitude of the pulsed channel. ✔ Cross talk < 0.002%

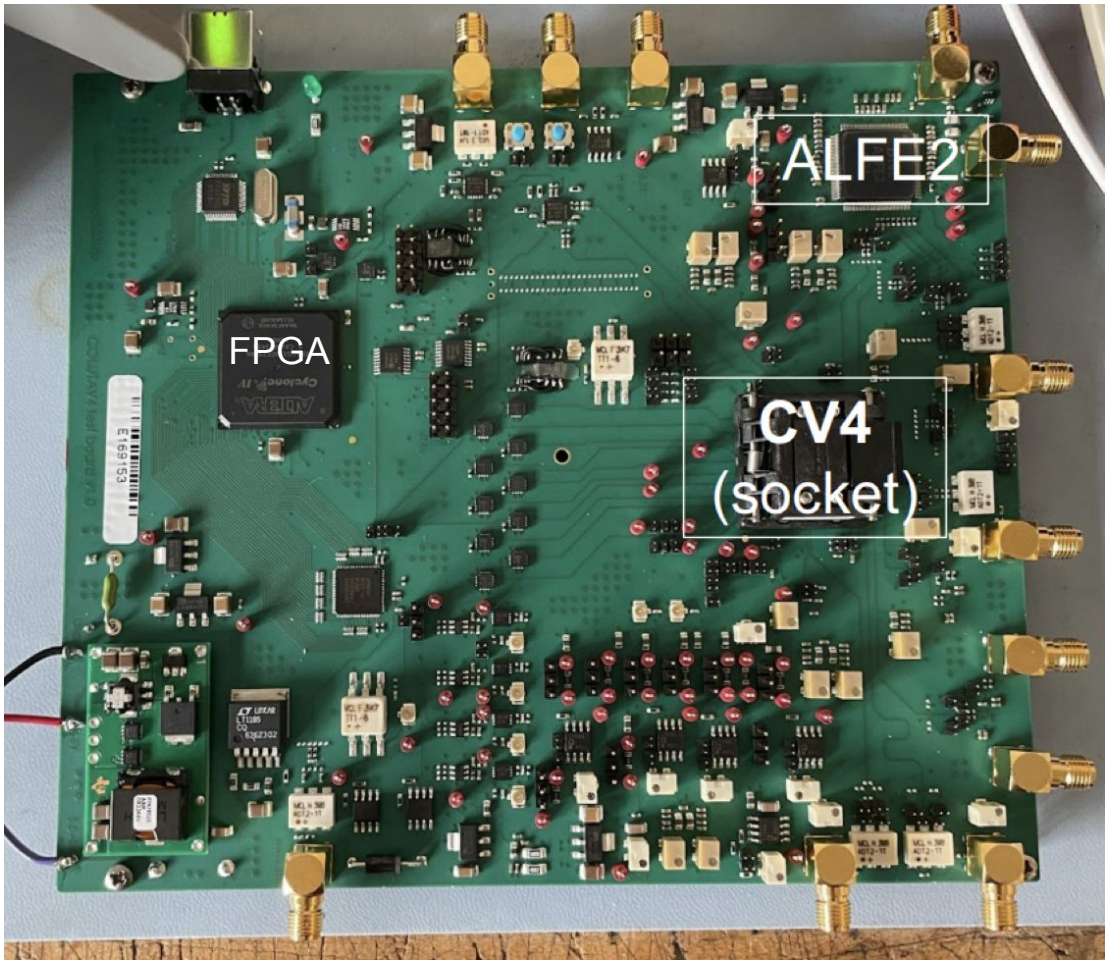
slide from FDR talk on COLUTA ADC: performance given by Eleanor Woodward

Block Diagram



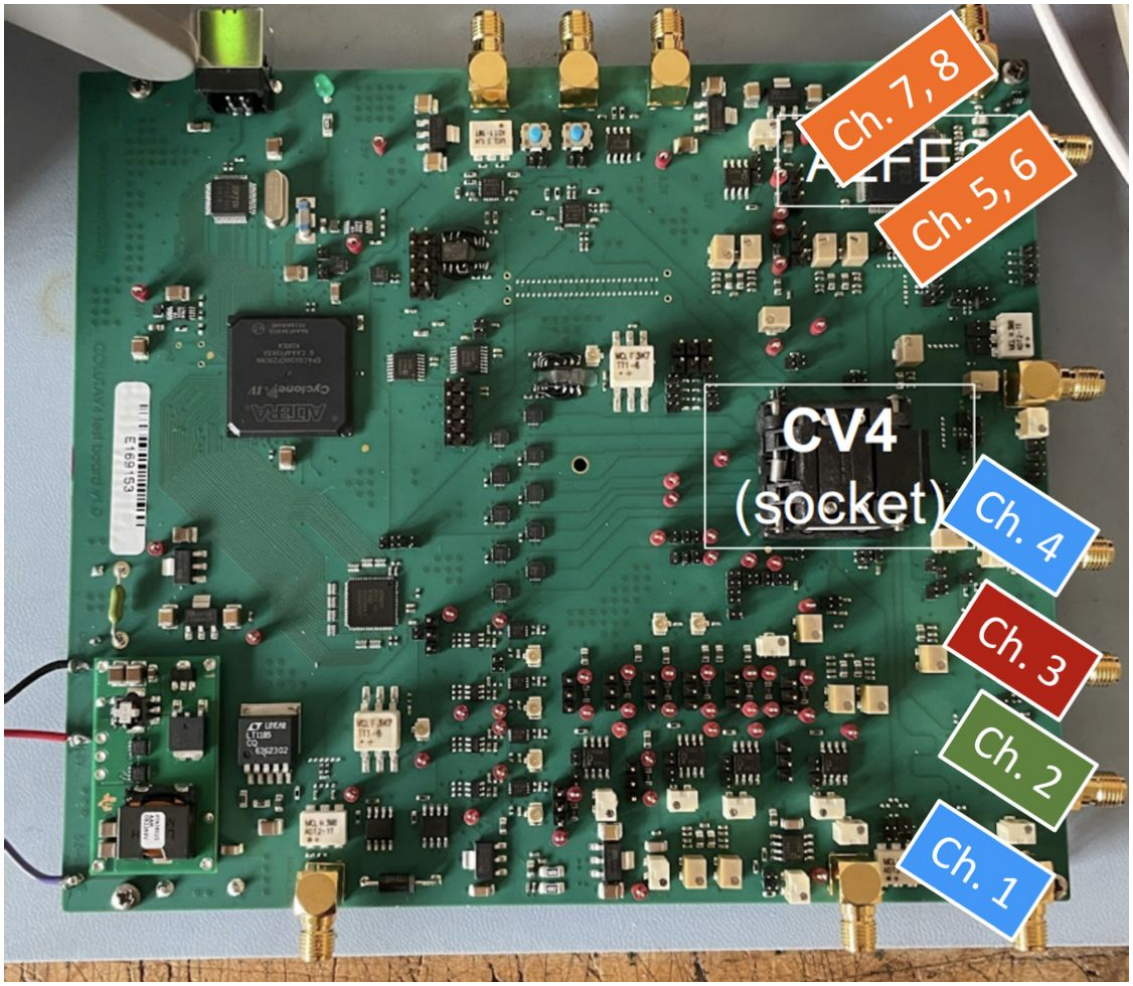
- for partial assembly:
  - 8 sets of ALFE2 + CV4 + associated CMS LDO + 24 lpGBT +8 VTRx+
- 128 channel / full assembly:
  - 32 sets of ALFE2 + CV4 + CMS LDO + 24 lpGBT + 8 VTRx+
- for more block diagrams:
  - https://twiki.nevis.columbia.edu/twiki/pub/ATLAS/SliceTestboard/FEB2_block_diagrams.pdf

testboard used for FDR



left is a plot of COLUTAV4 QFN packaged on the testboard used for preparing for the FDR

8 channels



left is the same board but includes the labelling of where the 8 channels are connected