COLUTAv4 Update

Tim Andeen, Associate Prof., UT Austin

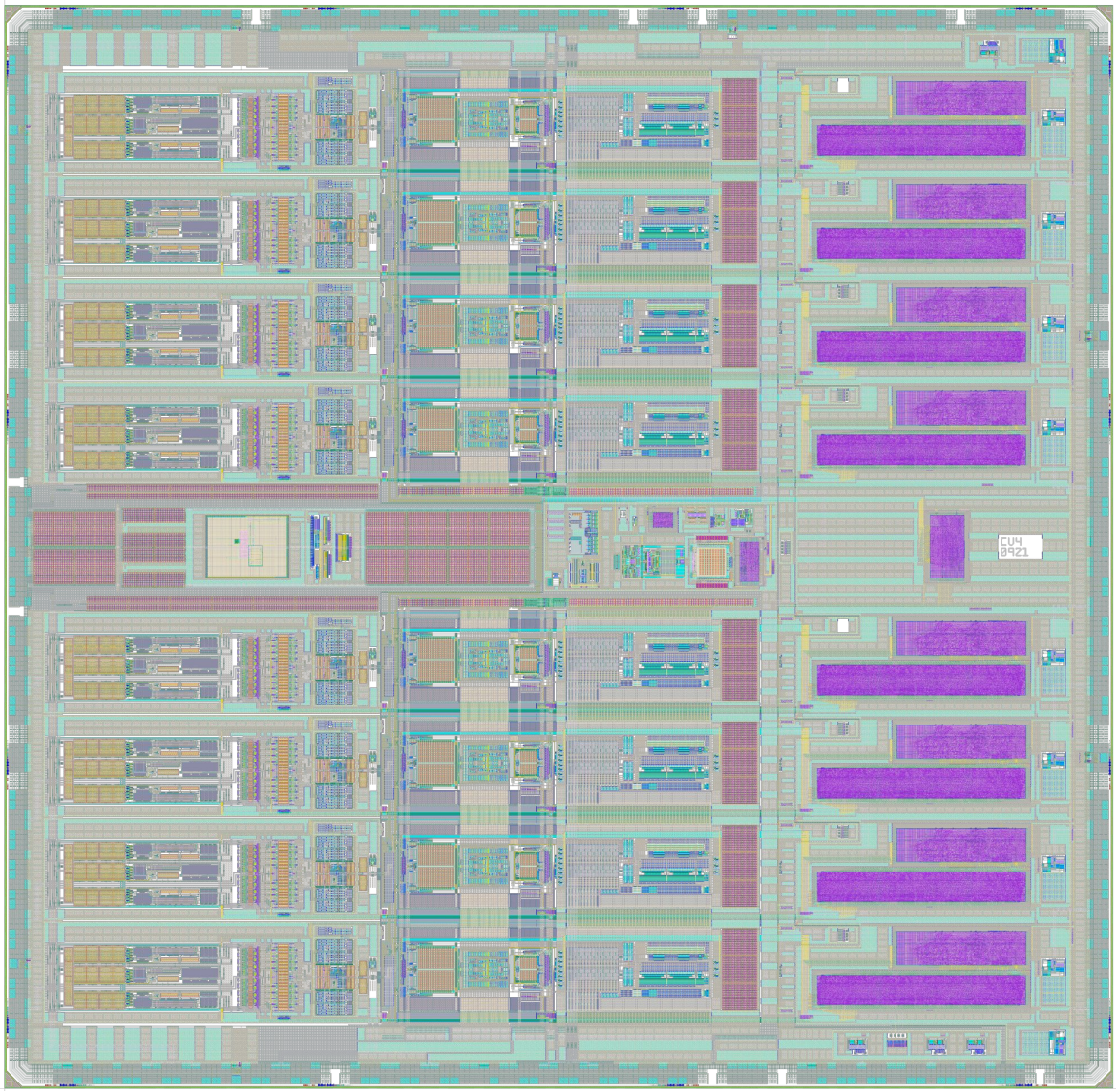
on behalf of the COLUTA Team

October 6, 2021

Introduction

- COLUTAv4 Status at submission
- Progress on packaging
- Progress on production test setup

COLUTAv4



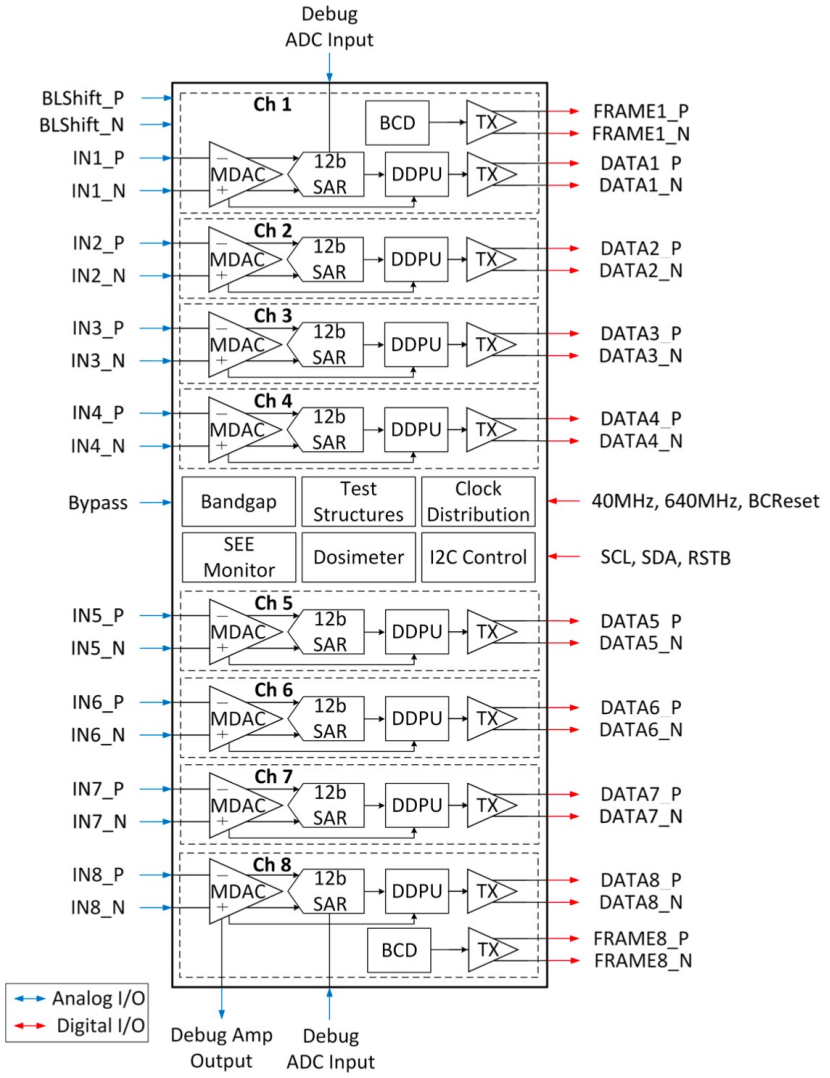
- **Submitted Sep. 1**

- TSMC 65nm LP 1.2 V
- 5.584 x 5.456 mm^2
- 100 I/O & 366 bondpads
- 4.3 million transistors

COLUTAv4

Prototype:

- 8 (identical) channel15b A/D
  - MDAC+SAR+DDPU
- Seamless interface to PA/SH chips
- Digital outputs, Clock signals, BC resets, and Controls are lpGBT compatible
- BC ID in the frame output
- On-chip band-gap derives all required analog voltages



COLUTAv4 Modifications

Several modifications from COLUTAv3 (following PDR recommendations)

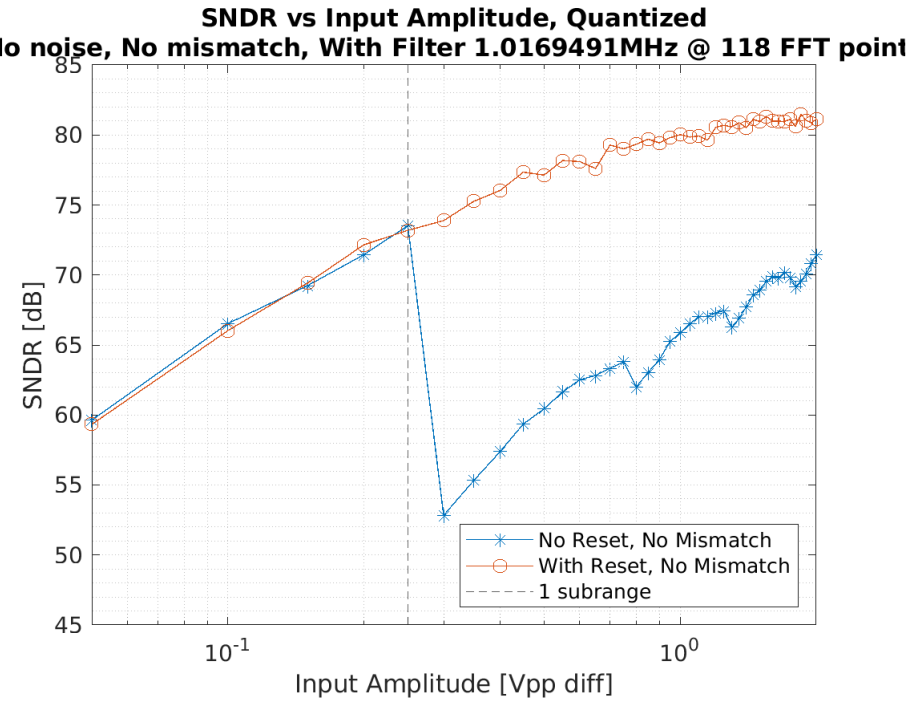
- Full discussion see Ray Xu's talk from Sep. 2 Phase-2 On-detector Mtg.

- **Analog settling** : Non-linearity as signal enters different MDAC subranges.
  - Mitigation - Extra (optional) clock phase was added into the MDAC to reset the sampling capacitor.
- **Analog settling** : Parasitic resistance results in insufficient reset leading to nonlinearity.
  - Mitigation - Reroute MDAC circuity to different metal layers. Verify in R+C+CC simulation.
- **Digital correction** : If the analog range was less than the correct 2^n factor then would have a discontinuity.
  - Mitigation - A sign bit was added to the MDAC correction for additional redundancy.
- **I2C**: "NO-ACK" systematically observed in radiation test board (and simulation) due to arbitrary timing relation between SCL and state machine's on-chip 40 MHz clock.
  - Mitigation - Schmitt trigger I/O pads used. CERN Microelectronics Group recognizes the issues and now strongly recommends Schmitt trigger for I/O pads.
- **SEE**: Further SEE mitigation in digital blocks.
  - Mitigation - Discussions with CERN CHIPS team: TMRG and new synthesis/P&R scripts were used in CV4. Enforces > 15 um linear distance spacing of redundant logic

COLUTAv4 Simulation

- **Simulation "breadth":** simulation should mimic measurement procedure.
  - Calibration simulation with on-chip digital arithmetic
  - Sine wave measurement with on-chip digital arithmetic
  - I2C functionality; Signal-in → signal-out
  - Depending on simulation goal, digital blocks may be simulated at the transistor level
- **Simulation "depth":** check sensitivity to R+C+CC parasitics.
  - Digital blocks: behavioral simulation → extracted P&R simulation
  - Analog blocks: schematic simulation → extracted R+C+CC simulation
- Putting it all together:
  - Full-chip extraction simulation possible with careful control of the design hierarchy.

Example: Pin-point simulation for analog settling



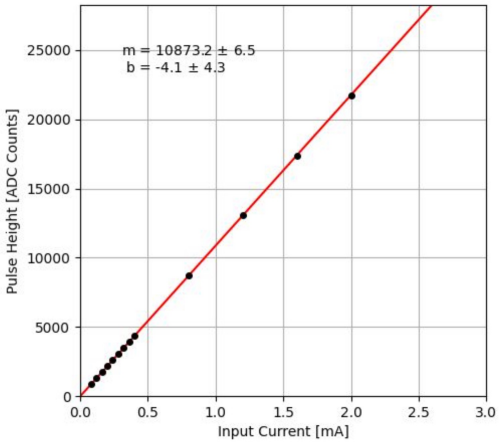
- Run **with** fix (**red**) and **w/o** fix (**blue**). Some simulation features left out (i.e. transient noise) for efficiency.
- Simulation mimics measurement procedure, closes loop between measurements (calibration, data acquisition).

See talk from Sep. 2 Phase-2 On-detector Mtg.

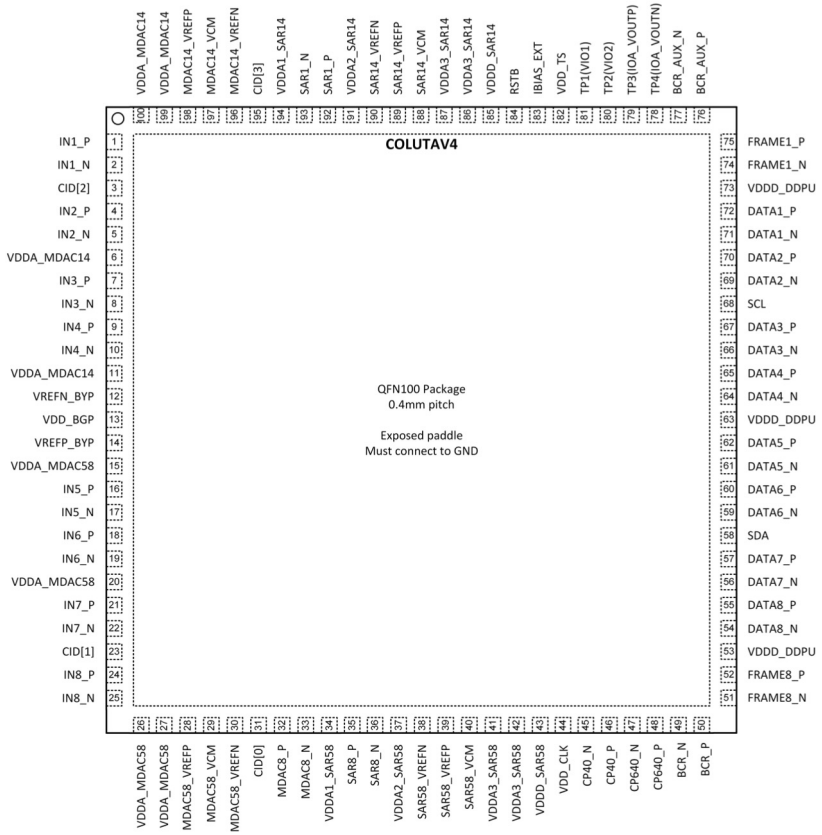
Integration

- PDR recommendation: Verify performance over power supply range 1.2 V±10%
  - Design choice to comprising maximizing full range while keeping transistors in saturation at nominal VDD of 1.2 V
    - maintain a fixed headroom (100 mV) w.r.t. VDD and GND.
  - **Impact:** PA/S and ADC should share a common 1.2V LDO to maintain the same full range (to avoid issues with radiation-induced drift in VDD). LDO output should be heavily filtered.

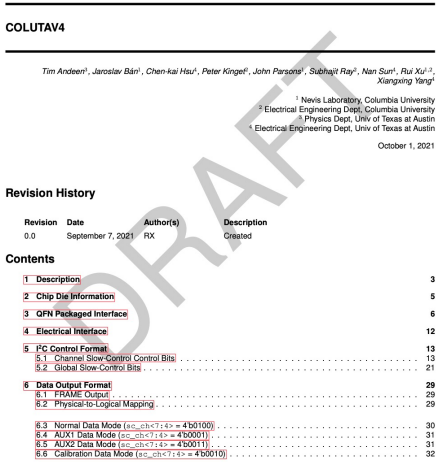
- PDR recommendation: Characterize PA/S+ADC
  - Used 32 ch. Slice Test Board (top right) to measure pulse shapes, energy/time resolution, INL (bottom right).
    - Many measurements done. See Andrew Smith's talk today.
  - Studied PA/S ADC interface in simulation (see Mietek's talk) and further transmission line simulations.



Packaging



- For initial test (early 2021) will use QFN100 package (QuikPak).
- Pinout prepared.
- Documented in (draft) datasheet.



COLUTAV4

Tim Andeen[1], Jaroslav Bán[1], Chen-kai Hsu[1], Peter Kinget[2], John Parsons[1], Subhajit Ray[3], Nan Sun[1], Rui Xu[1,2], Xiangxing Yang[1]

[1] Nevis Laboratory, Columbia University
[2] Electrical Engineering Dept, Columbia University
[3] Physics Dept, Univ of Texas at Austin
[4] Electrical Engineering Dept, Univ of Texas at Austin

October 1, 2021

DRAFT

Revision History

Revision	Date	Author(s)	Description
0.0	September 7, 2021	RX	Created

Contents

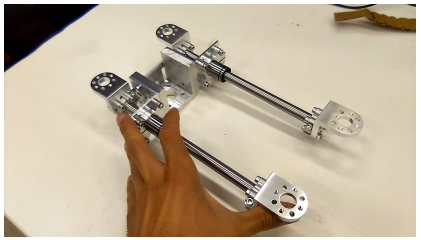
  - Includes SC bit assignments. (I2C)
  - *And* data output format (Frame, modes)
- BGA package quote (through CERN) in progress. Significant work already done. Plan to test in late(?) winter.

Testing

Preparing now for production testing of 80k chips.

- Coordinating plans between interested groups (UT Austin, Saclay and Nevis). See Sep. 30 Phase-2 ADC meeting.
  - **Austin**: Assembling robotic arm setup. In contact with Lund ALICE group ("SAMPA" robot). Interfacing existing test software to automate measurements.
  - **Saclay:** Experience with COLUTAv2 testboard and software. Existing "Pacman" automated robotic ASIC testbench.
  - **Nevis:** Existing test setups, including Slice test board.

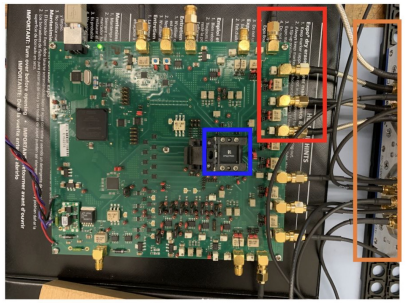
UT Austin:



Yamaha YK500XGL

Saclay:

Nevis:



Socket + ASIC
Programmable Switch
MDAC Channels (5-8)

Closing Remarks

- COLUTAV4 builds on the successes of previous versions
  - Eight MDAC+SAR channels; final prototype ADC following series of 3 pre-prototypes
  - 5.584 x 5.456 mm^2 ; 4.3 million transistors
- Largest and most complex chip to date in the COLUTA group
  - Most extensive simulation & verification effort so far.
- We look forward to testing V4!
  - Submitted Sept 1st
  - Chip dies expected back early December of this year.
- Many efforts happening in parallel (packaging, testing, firmware, software)
- We look forward to your comments.

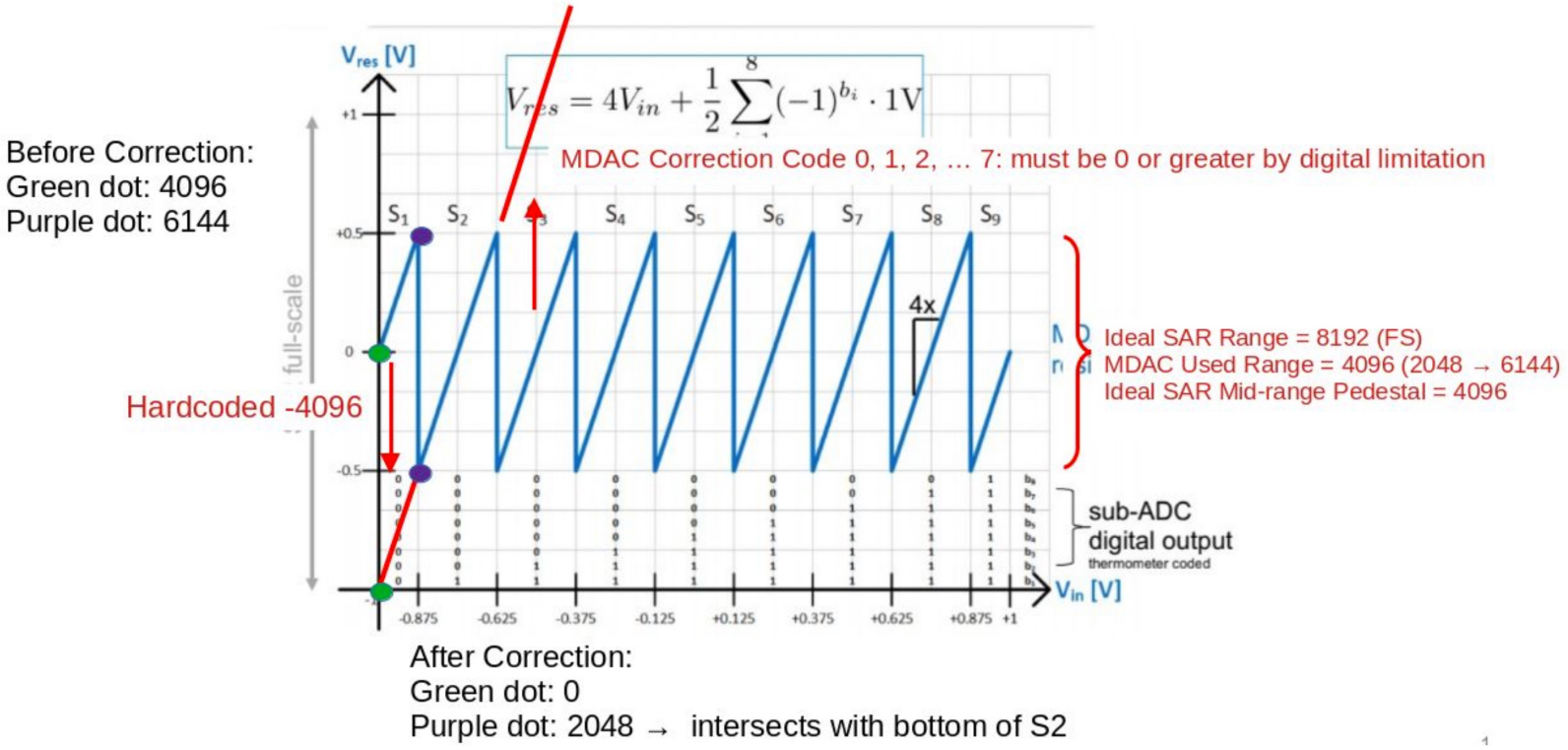
ATLAS EXPERIMENT

BACKUP

Modification: Digital Correction

- Ideal case: analog range is exactly equal to the radix-2 designed values

Ideal DDPU Correction, No Redundancy

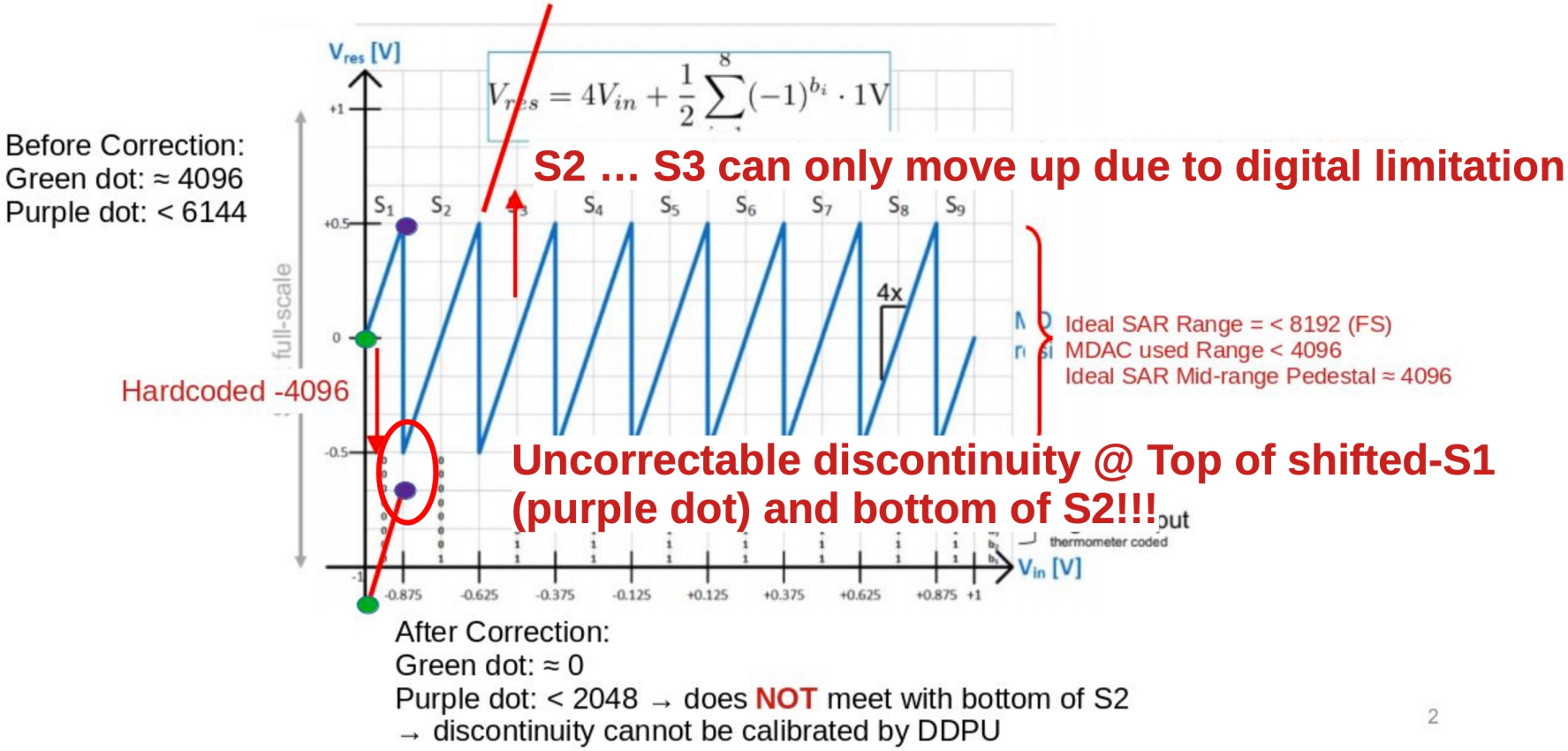


See talk from Sep. 2 Phase-2 On-detector Mtg.

Modification: Digital Correction

- Scenario: analog range is slightly less than the radix-2 designed values

Actual DDPU Correction, No Redundancy

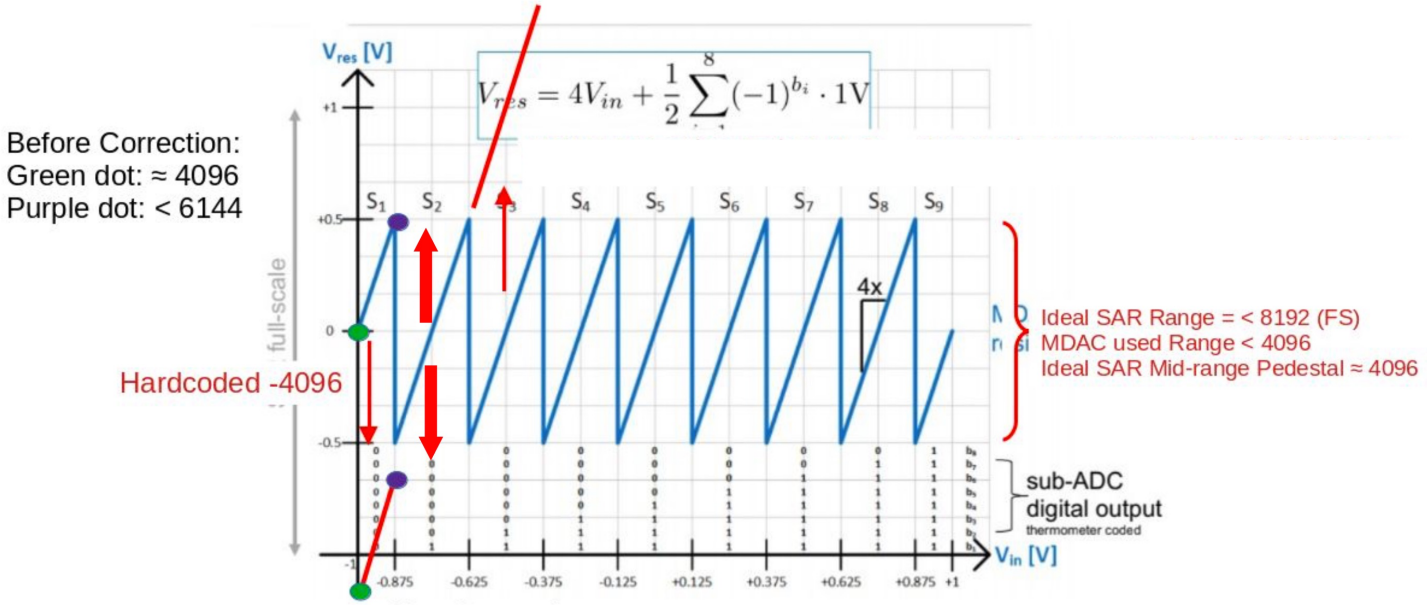


See talk from Sep. 2 Phase-2 On-detector Mtg.

Modification: Digital Correction

- Fix: Allow programmability in the MSB of correction constant S2. In two's complement, this is the sign bit. Allows S2 to move up **or** down.

Actual DDPU Correction,



By allowing S2 to move up or down, the DDPU digital code output will be continuous. S2 will have a programmable range equal to twice the designed range.

See talk from Sep. 2 Phase-2 On-detector Mtg.