COLUTAv4 Update

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March 16, 2022

on behalf of the COLUTA Team

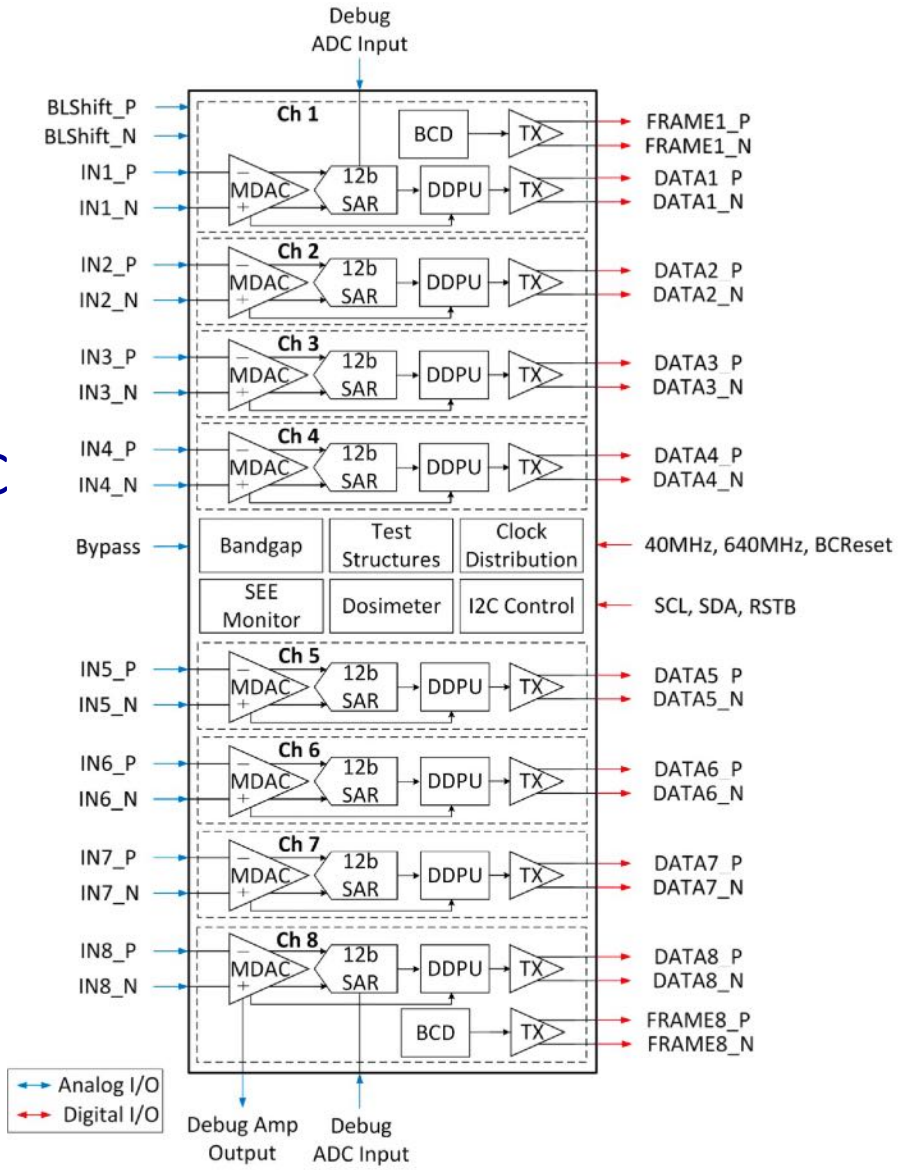
Introduction

1. COLUTAv4 overview
2. First test results
3. Progress on packaging, and production and radiation testing

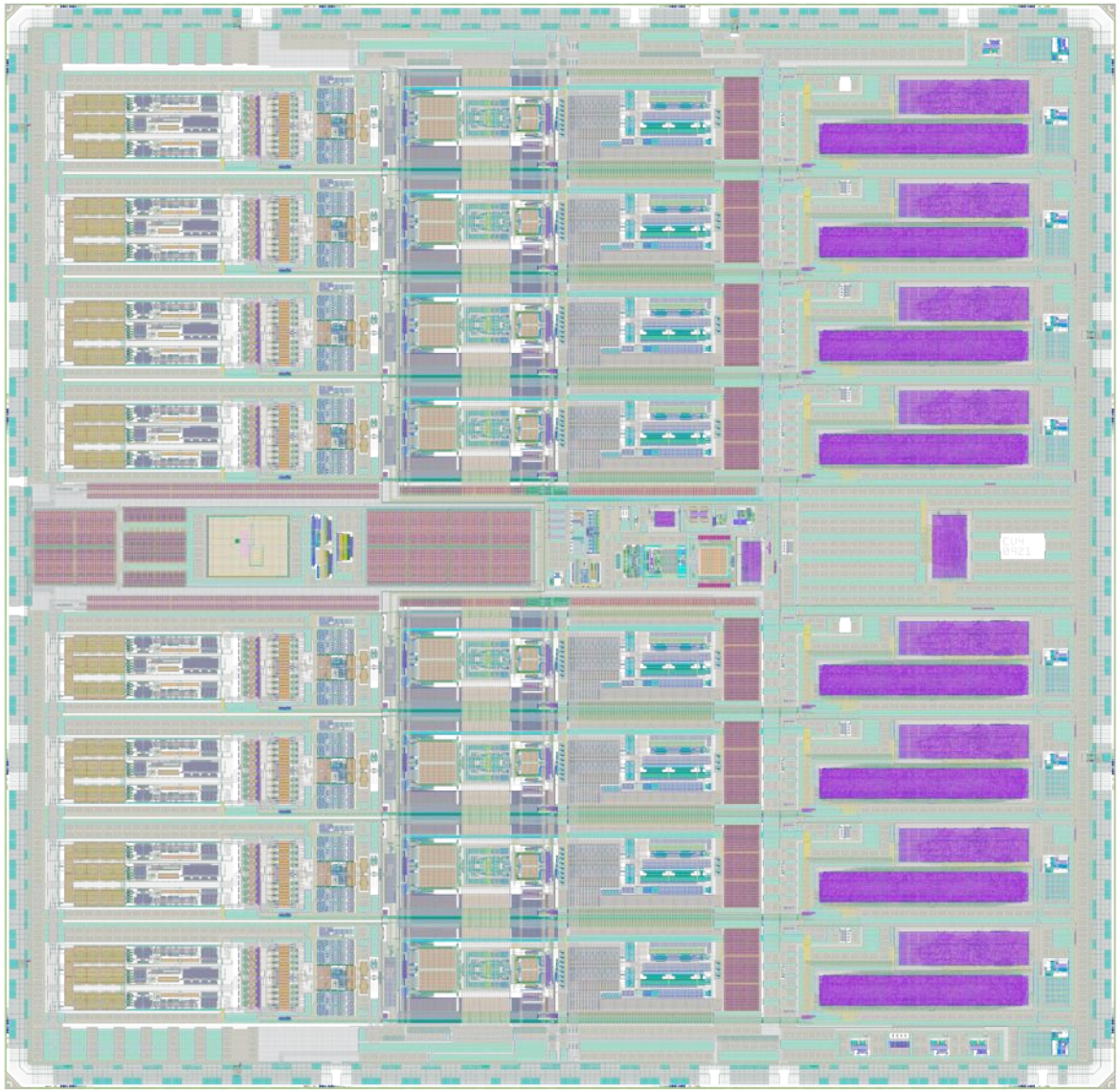
COLUTAv4

Prototype:

- 8 (identical) channel, 15b A/D
  - MDAC+SAR+DDPU
- Seamless interface to PA/SH chips
- Digital outputs, Clock signals, BC resets, and Controls are lpGBT compatible
- BC ID in the frame output
- On-chip band-gap derives all required analog voltages



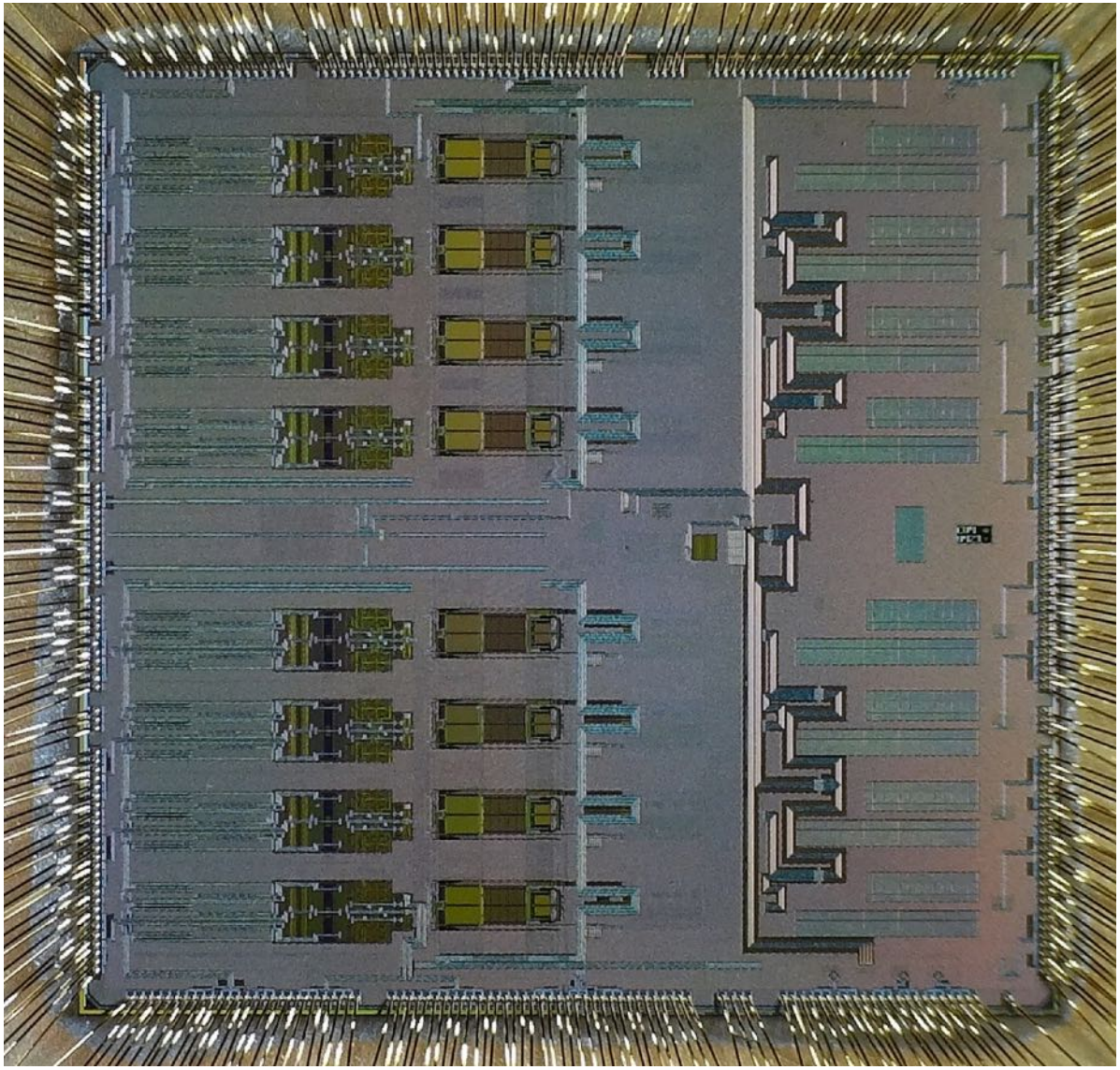
COLUTAv4



- **Submitted Sep. 1st**

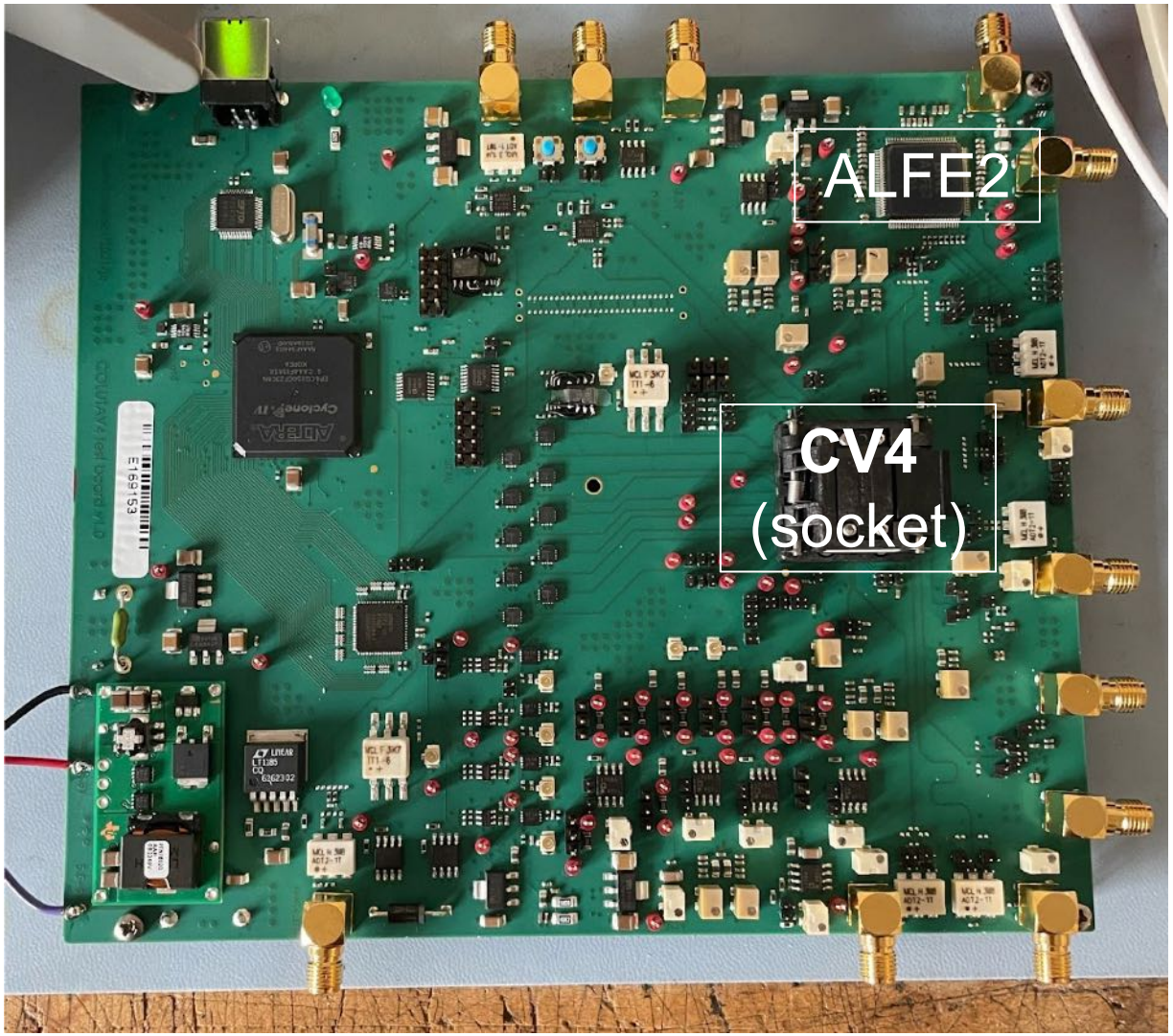
- TSMC 65nm LP 1.2 V
- 5.584 x 5.456 mm^2
- 100 I/O & 366 bondpads
- 4.3 million transistors

COLUTAv4



- **Received Dec. 20th**
  - With help from Luis
- Packaged in QFN100 by QuikPak.

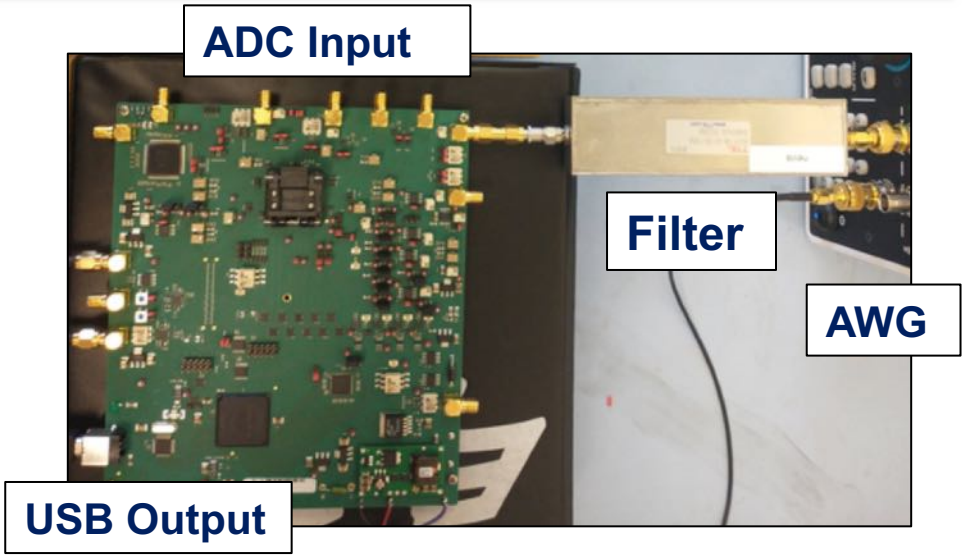
Testboard

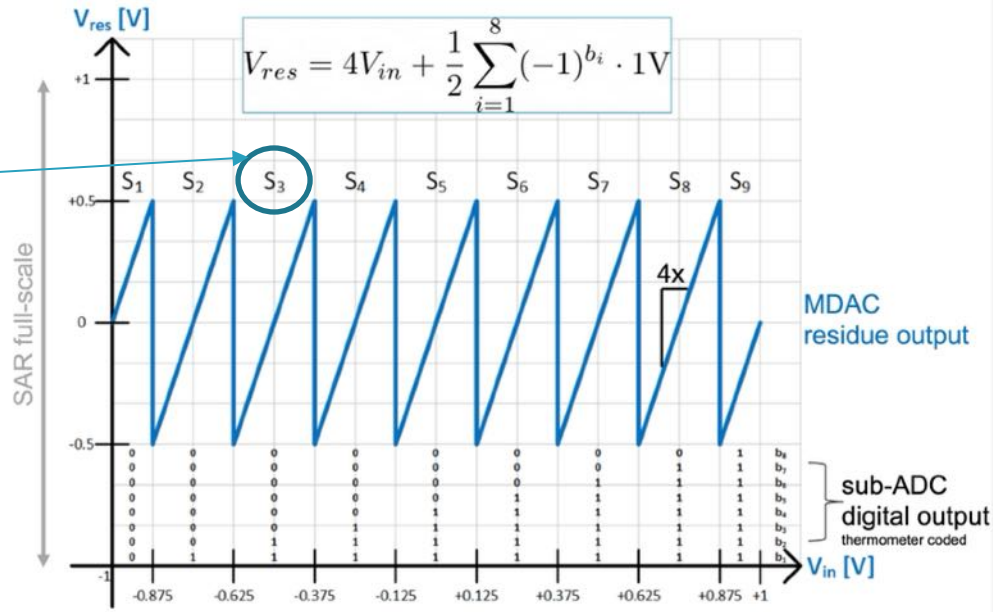


- Board fabricated and assembled mid-Jan through early-Feb.
- Testing started **Feb. 22nd.**
  - Socketed board for initial testing. Option to solder down.
  - Includes ALFE2 chip for integrated testing with PA/SH. Not included in testing for this talk.

Test Setup and Calibration

- Initial tests done with one chip, one channel.
  - Signal provided by Arbitrary Waveform Generator (AWG), with filters (for sine wave) and attenuators.
    - Connected directly to board.
- Calibration of MDAC and SAR done offline
  - Maximize bit-weights (S_i in MDAC) for best possible ENOB.
  - Allows us to separate investigation of analog circuit performance from digital perf.
    - On-chip calibration tested, full results in progress.



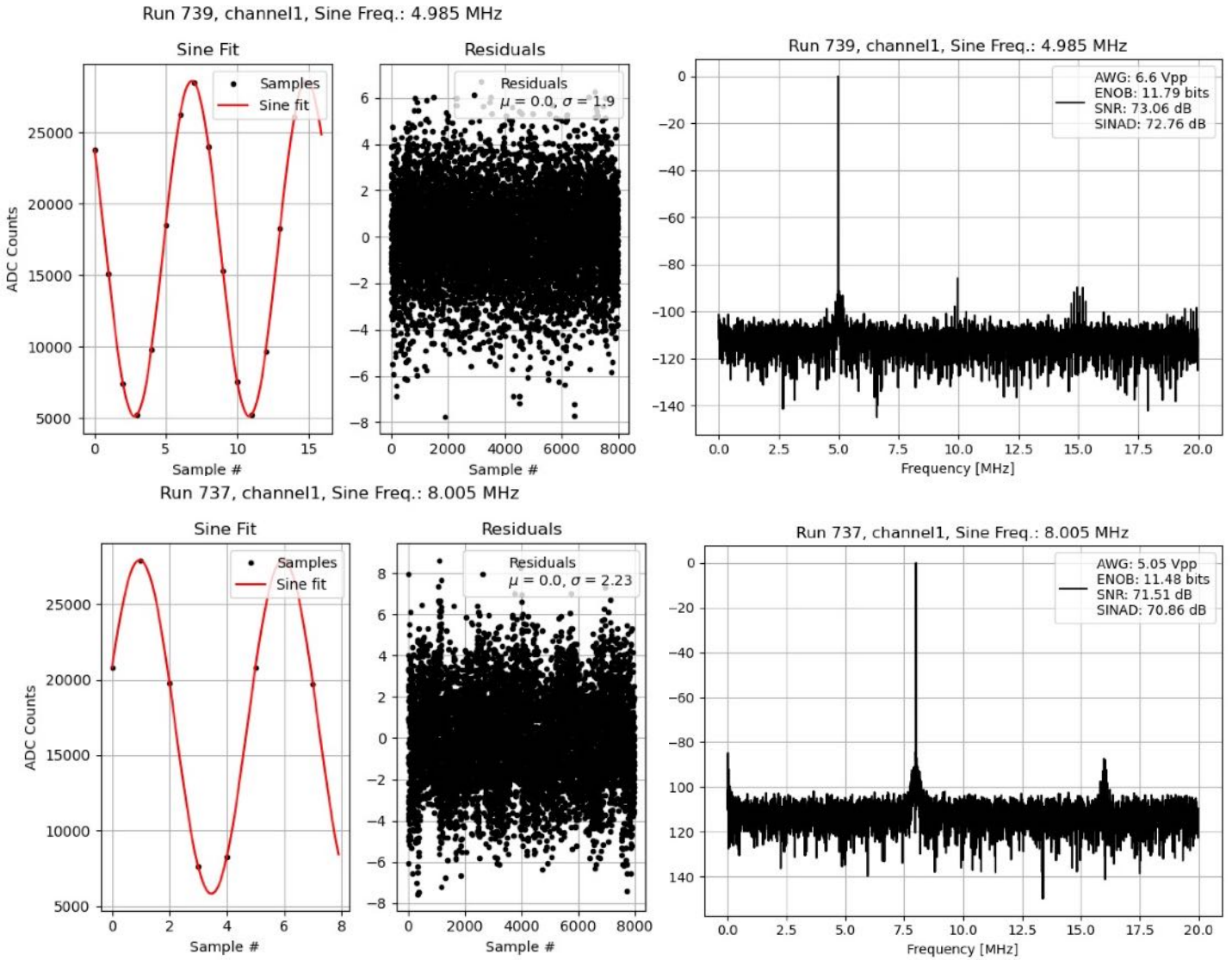


Initial Test Results

Sine Wave Performance

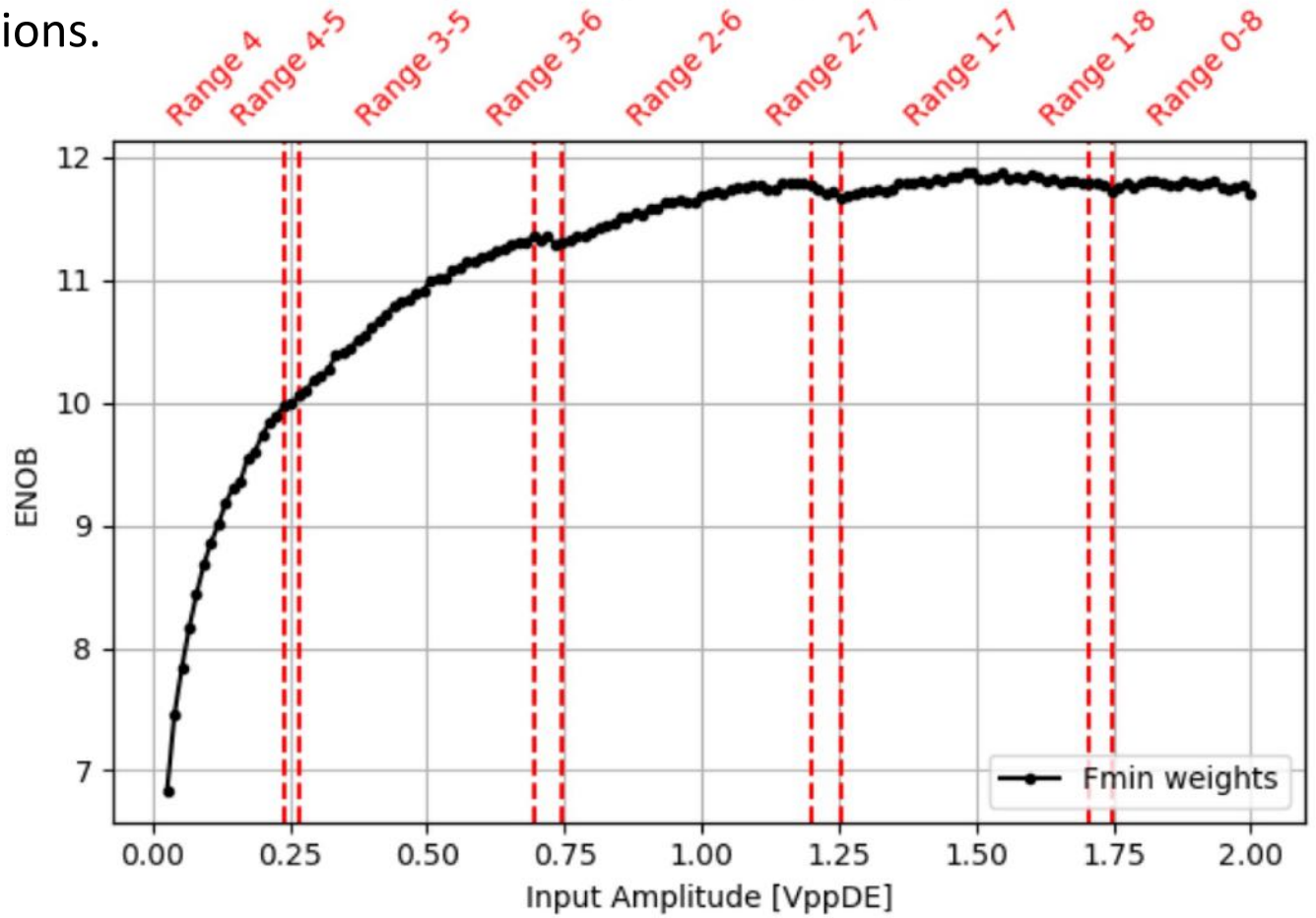
Channel 1 w/ 5 and 8 MHz sine wave signals, calibration done off-chip.

- Signal fitted to sine function (red) with residuals shown in middle plot.
- FFT >11b at close to full-scale.



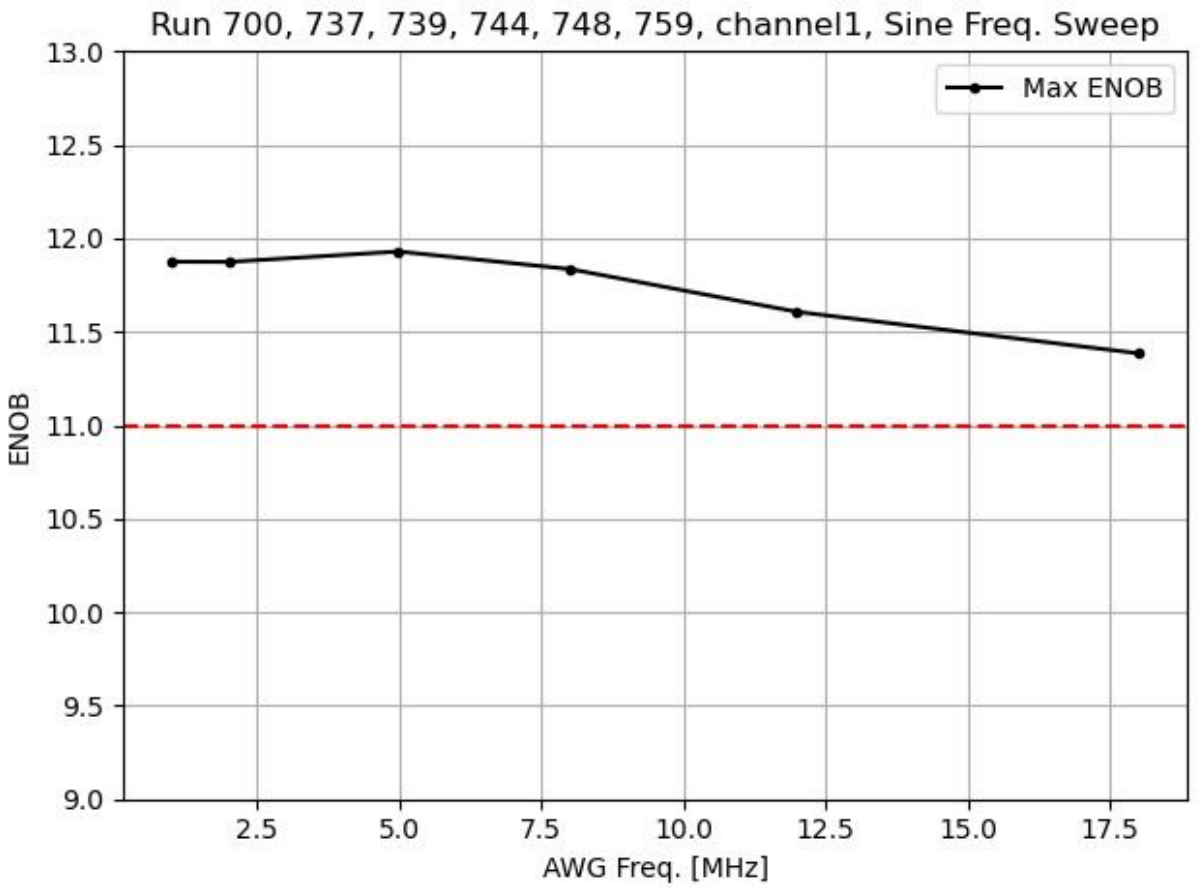
ENOB vs Amplitude

- Vary amplitude of sine wave signal to scan performance. ENOB > 11b for V_{pp} > 0.5 V.
  - Offline calibration allows us to check specific MDAC ranges and transitions.



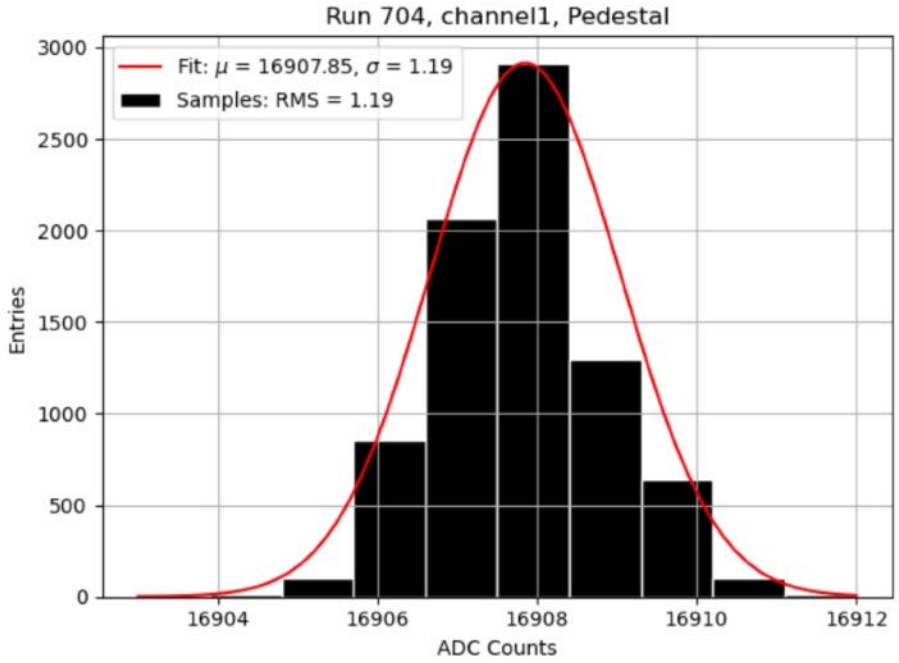
ENOB vs Signal Freq.

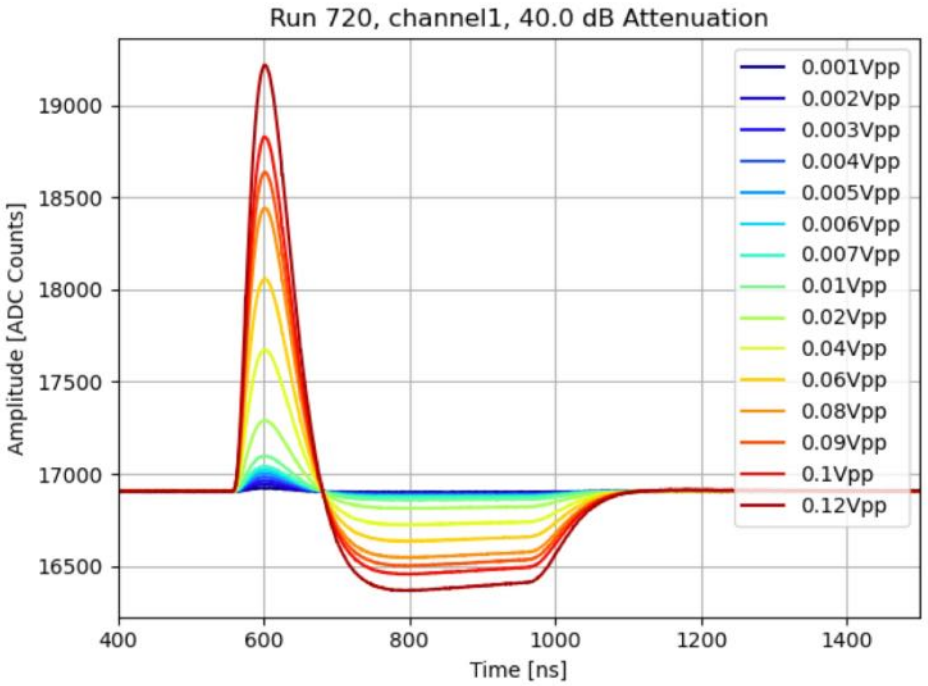
- With sine wave with fixed amplitude (close to full-scale), vary signal frequency from 1 to 18 MHz (~Nyquist).
  - Performance specified at 8 MHz.
  - ENOB > 11b up to 18 MHz.



Pedestal and LAr Pulse

- Check pedestal noise, 1.2 ADC counts RMS (left)
- Moving on from sine wave signals, check LAr pulse in CV4 (right)
  - 30 pulses interleaved to create fine resolution pulse for analysis (OFCs)
  - To come: energy and time resolution performance

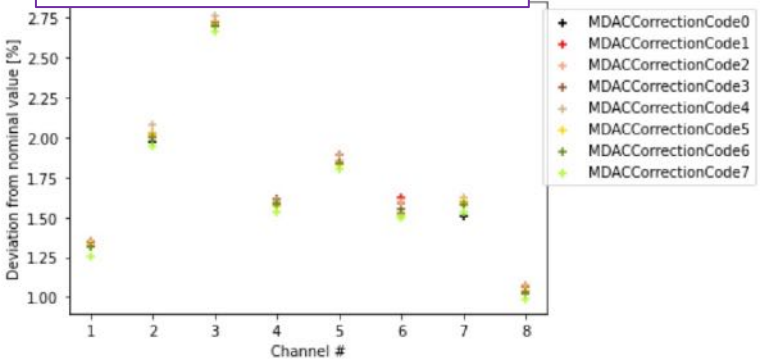




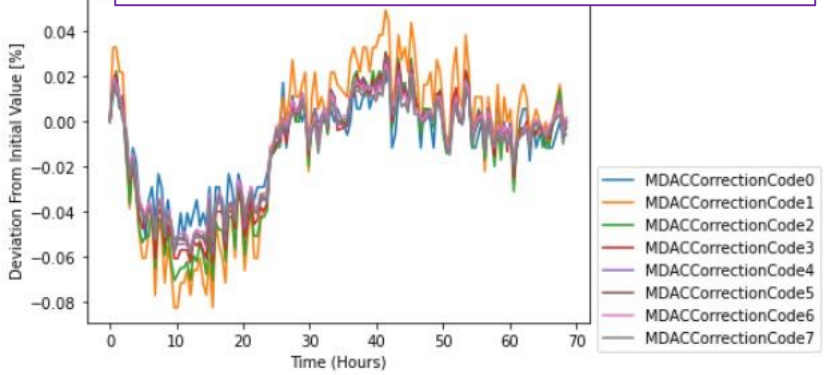
Stability Overtime

- First look at on-chip calibration and calibration stability.
  - Left: single measurement of weights in MDAC and SAR by channel.
  - Right: monitor weights (top right: MDAC, bottom right: SAR) on each channel over a multi-day data-taking run (at ambient temp/humidity/etc.).

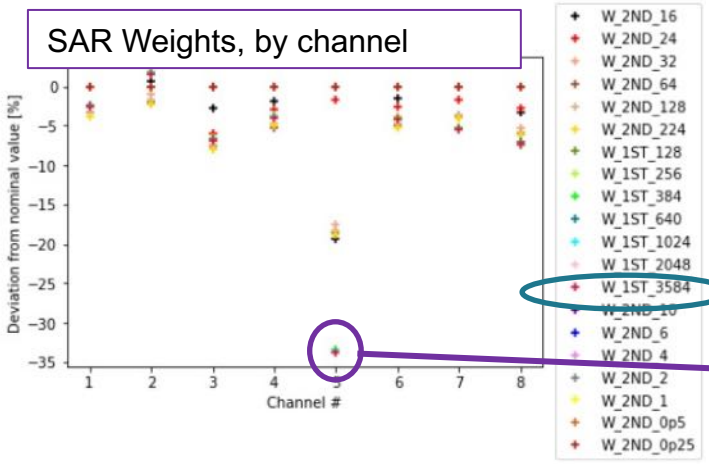
MDAC Weights, by channel



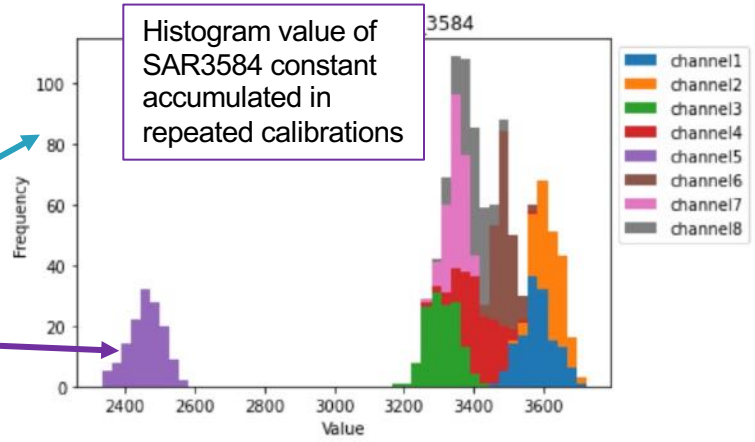
Change in MDAC Weights (Ch 8)



SAR Weights, by channel

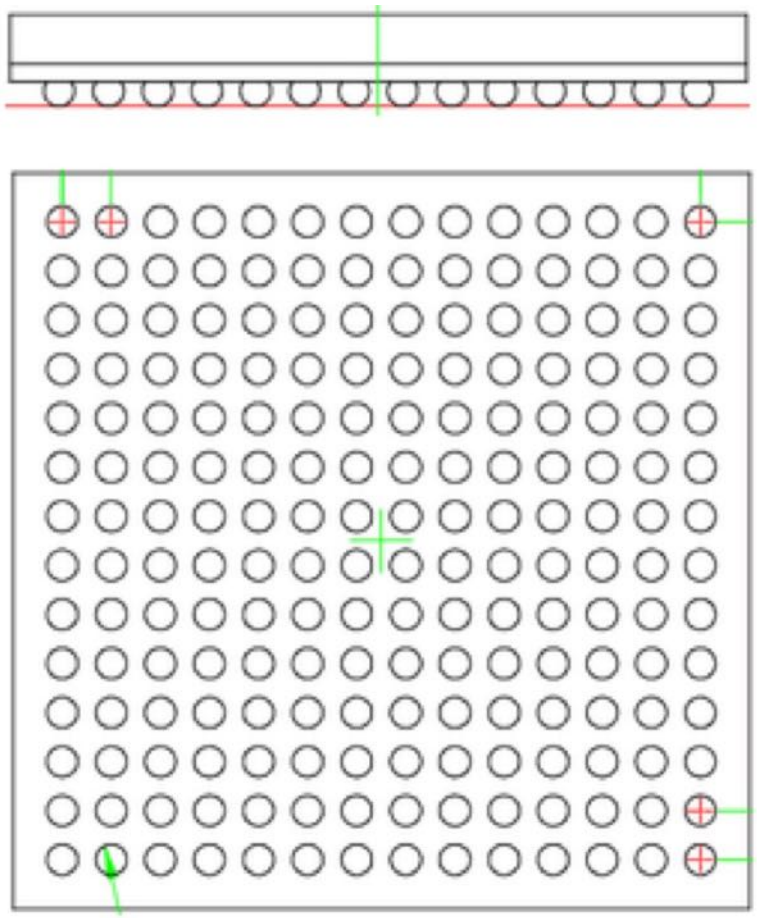


Histogram value of SAR3584 constant accumulated in repeated calibrations



Packaging & Radiation/Production Testing

Packaging



- BGA package waiting for quotes from vendors.
  - Review bids this Friday (March 18).
- BGA packaging specifications
  - Low profile fine pitch BGA
  - Ball pitch: 0.8 mm
  - Size: 12 x 12 mm
  - Pin count: 196
- If packaging vendor is the same as ALFE, can coordinate on test sockets.

Production Testing

Preparing now for production testing of 80k chips.

- Coordinating plans between interested groups (UT Austin, Saclay and Nevis).

- **Austin**: Assembling robotic arm setup. Interfacing existing test software to automate measurements.
- **Saclay:** Preparing to send COLUTAv4 test board to Saclay. Existing robotic test setup being prepared for ADC testing.
- **Nevis:** Experience with existing test setups and measurements.

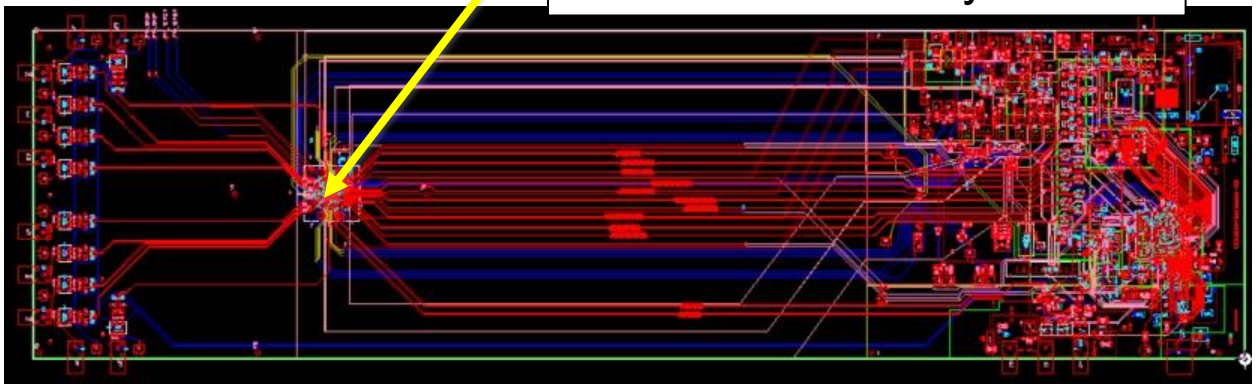
UT Austin: Long duration tests (over a weekend) checking placement of "dummy" chips.

Radiation Testing

Radiation testing scheduled for June 4/5 at MGH (Boston)

- Board design in progress, anticipate submitting for fabrication soon.
  - Follows CV3 design.
  - Focus on SEE tests -> Verify improved SEE mitigation in digital blocks with new, larger spacing for redundant logic.
- Exploring possibility for testing at Fermilab's ITA.
  - Tight schedule, their beam shuts down in July for ~3 months.

CV4 Rad. board layout

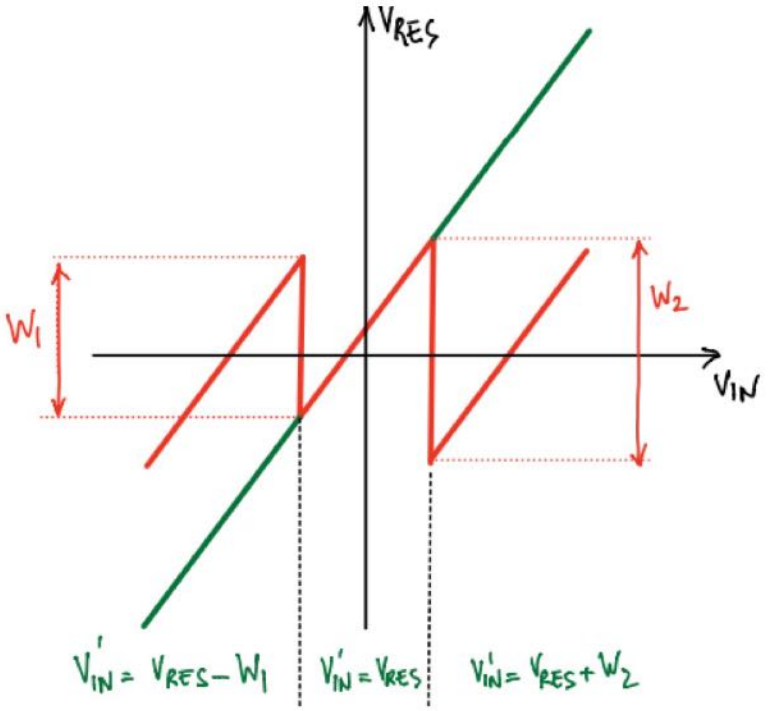


Closing Remarks

- Testing COLUTAV4 in progress.
  - Initial results are promising. Many measurements to make in the next weeks/months.
  - Radiation testing planned for June 4/5.
  - Now that (most of) functionality of the 2 testboards validated, ship one to UT Austin and assemble another one to ship to Saclay for additional testing.
- COLUTAV4 builds on the successes of previous versions
  - Eight MDAC+SAR channels; final prototype ADC following series of 3 pre-prototypes
  - 5.584 x 5.456 mm^2 ; 4.3 million transistors
- Largest and most complex chip to date in the COLUTA group
  - Most extensive simulation & verification effort so far.
- Many efforts happening in parallel (packaging, testing, firmware, software, data sheet documentation).

BACKUP

Foreground Calibration Principle



Simplified diagram for three sub-ranges; chip has 9 sub-ranges and 8 W-constants

- Given a piece-wise linear transfer curve with the same gain in all sections and given the heights of the transitions W_i, you can reconstruct a linear V'_{IN} from the residue V_{RES}
  - V'_{IN} gain and offset error will be corrected by system

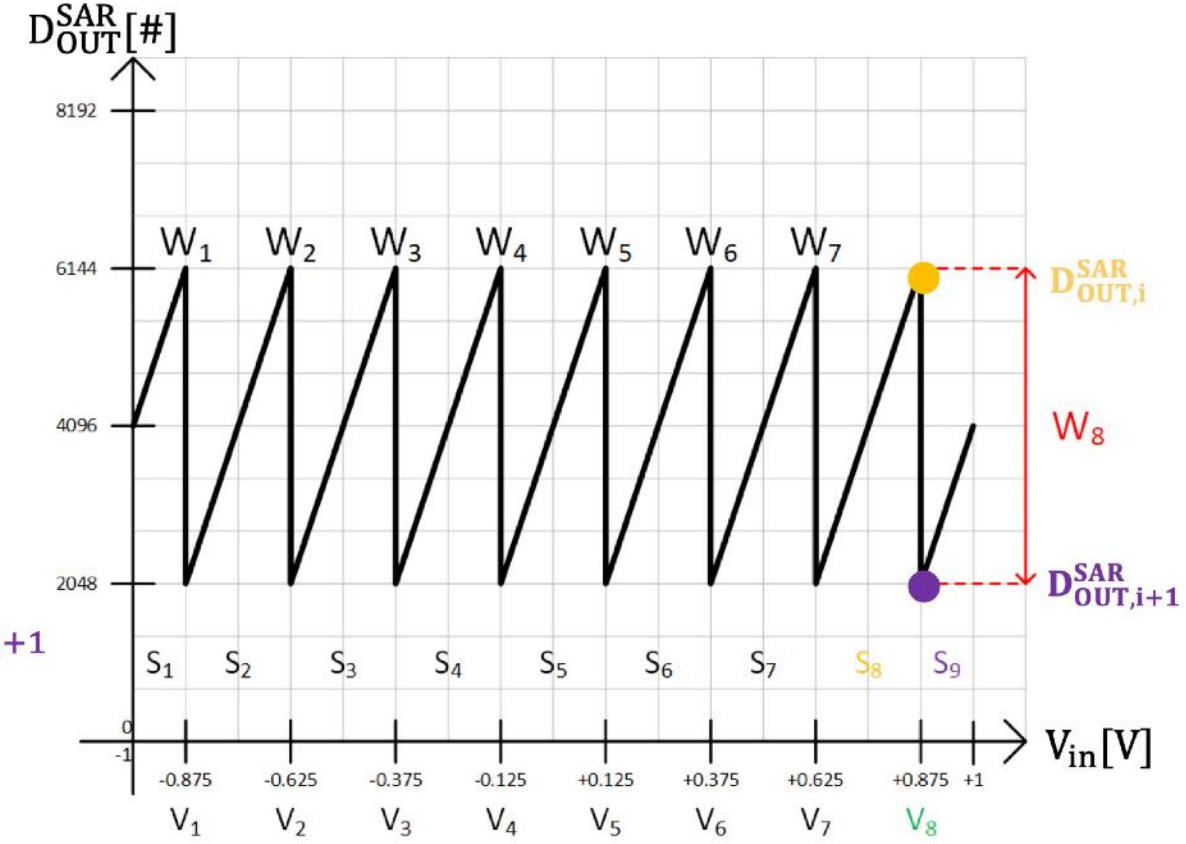
MDAC Calibration

Procedure

1. Assert V_i
2. Force S_i

carried out by calibration circuit

3. Measure $D^{SAR}_{OUT,i}$
4. Force S_{i+1}
5. Measure $D^{SAR}_{OUT,i}$
6. Calculate $W_i = D^{SAR}_{OUT,i} - D^{SAR}_{OUT,i+1}$
7. Repeat for i = 1 to 8

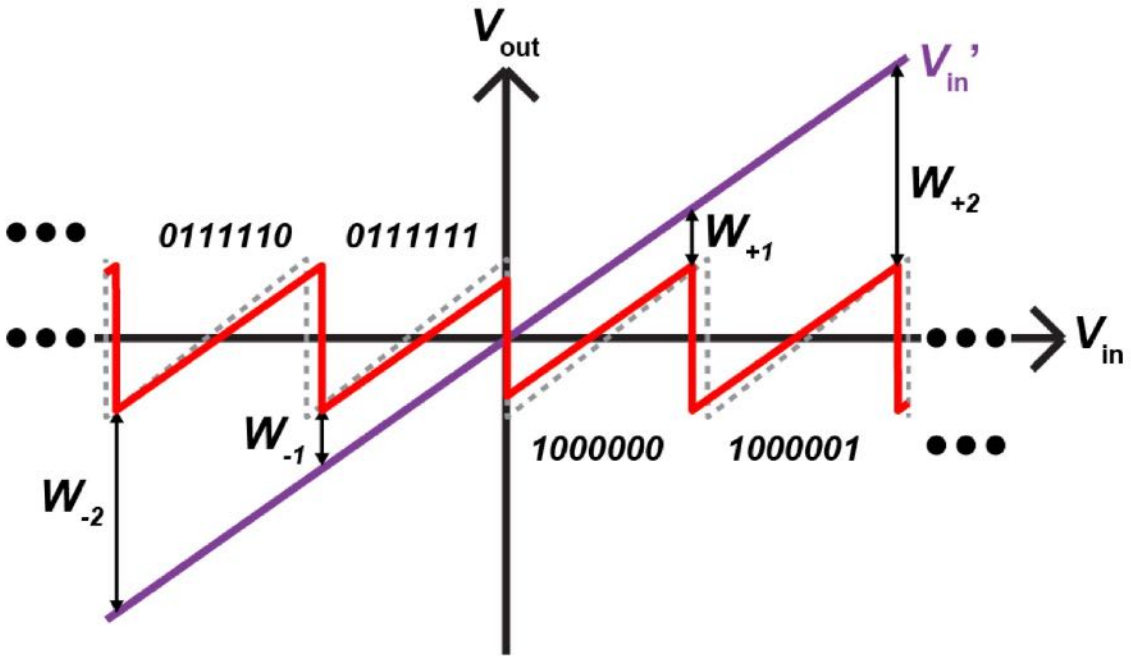


- DDPU uses $W_1,\ldots,W_8$ to "stitch together" the segments:
- All circuitry to extract calibration constants is on chip
- MDAC calibration is done after SAR calibration

$$D_{out}^{MDAC+SAR} = D_{out}^{SAR} - 4096 + \sum_{i=1}^{8} W_i \cdot b_i$$

SAR Calibration

- Extract …W_{-1}, W_{+1}, W_{+2}, … so that linear V_{in}' can be reconstructed:
  - $W_{+1} = -[(-1)^1 A_{inter} V_{DAC}(7) + (-1)^0 A_{inter} V_{DAC}(6) + \cdots + (-1)^0 A_{inter} V_{DAC}(2) + (-1)^0 A_{inter} V_{DAC}(1)]$
  - $W_{+2} = -[(-1)^1 A_{inter} V_{DAC}(7) + (-1)^0 A_{inter} V_{DAC}(6) + \cdots + (-1)^0 A_{inter} V_{DAC}(2) + (-1)^1 A_{inter} V_{DAC}(1)]$
  - $W_{-1} = -[(-1)^0 A_{inter} V_{DAC}(7) + (-1)^1 A_{inter} V_{DAC}(6) + \cdots + (-1)^1 A_{inter} V_{DAC}(2) + (-1)^1 A_{inter} V_{DAC}(1)]$
  - $W_{-2} = -[(-1)^0 A_{inter} V_{DAC}(7) + (-1)^1 A_{inter} V_{DAC}(6) + \cdots + (-1)^1 A_{inter} V_{DAC}(2) + (-1)^0 A_{inter} V_{DAC}(1)]$



CV3 Modifications

Several modifications from COLUTAv3

- Full discussion see Ray Xu's talk from Sep. 2 Phase-2 On-detector Mtg.

- **Analog settling** : Non-linearity as signal enters different MDAC subranges.
  - Mitigation - Extra (optional) clock phase was added into the MDAC to reset the sampling capacitor.
- **Analog settling** : Parasitic resistance results in insufficient reset leading to nonlinearity.
  - Mitigation - Reroute MDAC circuity to different metal layers. Verify in R+C+CC simulation.
- **Digital correction** : If the analog range was less than the correct 2^n factor then would have a discontinuity.
  - Mitigation - A sign bit was added to the MDAC correction for additional redundancy.
- **I2C**: "NO-ACK" systematically observed in radiation test board (and simulation) due to arbitrary timing relation between SCL and state machine's on-chip 40 MHz clock.
  - Mitigation - Schmitt trigger I/O pads used. CERN Microelectronics Group recognizes the issues and now strongly recommends Schmitt trigger for I/O pads.
- **SEE**: Further SEE mitigation in digital blocks.
  - Mitigation - Discussions with CERN CHIPS team: TMRG and new synthesis/P&R scripts were used in CV4. Enforces > 15 um linear distance spacing of redundant logic

ENOB vs Signal Freq.

- ENOB > 11b up to Nyquist frequency
  - With on-chip calibration – improvements in progress