COLUTAV4

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Revision History

Revision	Date	Author(s)	Description
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1 Description

The COLUTAV4 device is an 8-channel, precision analog-to-digital converter (ADC) intended for instrumentation readout in radiation-prone areas with an emphasis on mitigating single-event effects. Each channel is intended for operation at 40MSPS and provide $\geq$11 ENOB SNDR. All channels are identical and feature a multiplying-DAC (MDAC) in the front-end coupled to an identical successive approximation register (SAR) ADC back-end. The chip is designed in TSMC's 65nm LP 1-poly 6-metal CMOS process.

This device is currently intended for use in the HL-LHC LAr Calorimeter Phase-II upgrade [1].

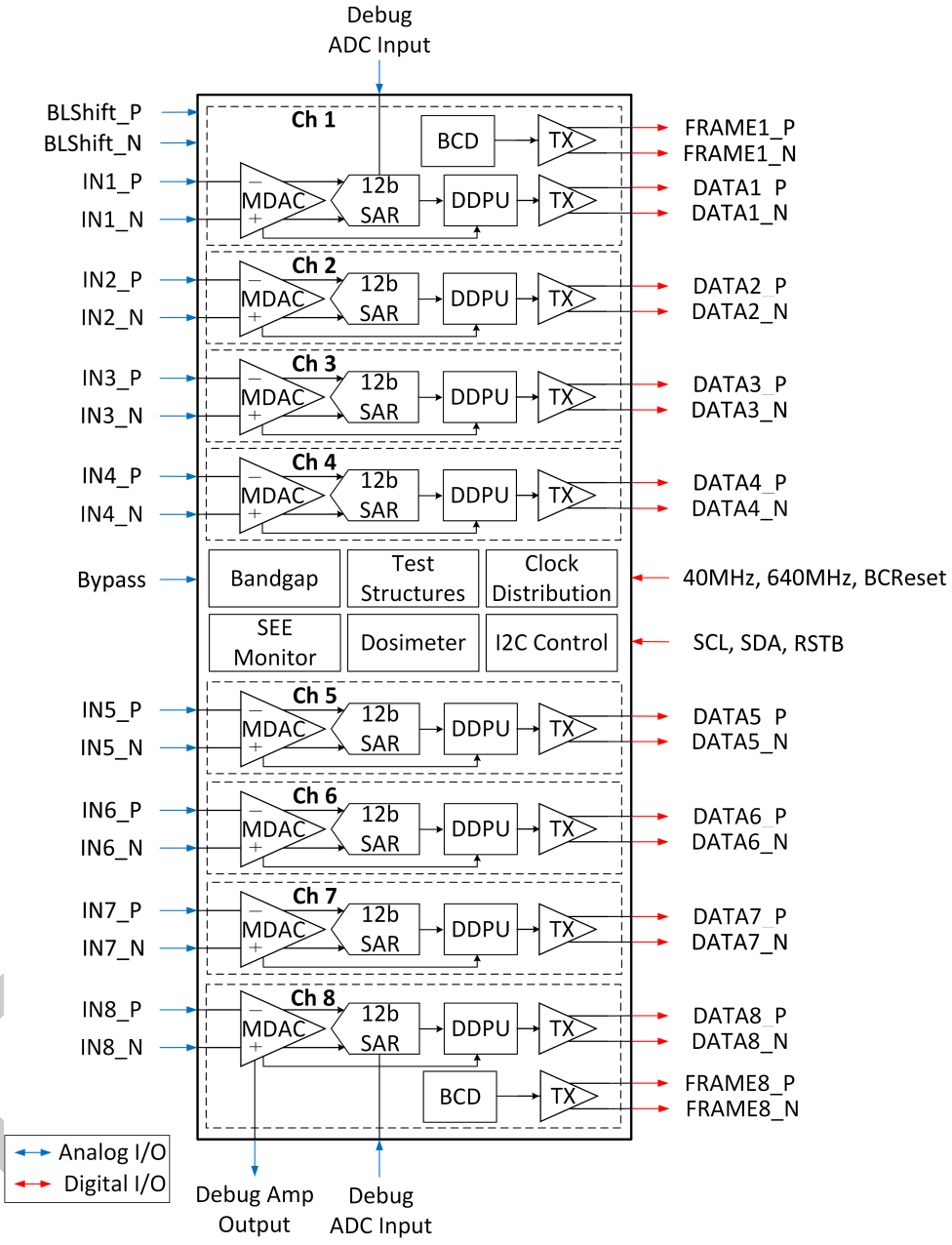

Figure 1: COLUTAV4 functional block diagram

2 Chip Die Information

The chip die measures 5.456mm x 5.854mm with single-in-line wirebonding pads along the periphery. A logo with the letters “CV4 0921” exists on the right-half, mid-height on the chip die. The chip contains a total of 4.3 million transistors.

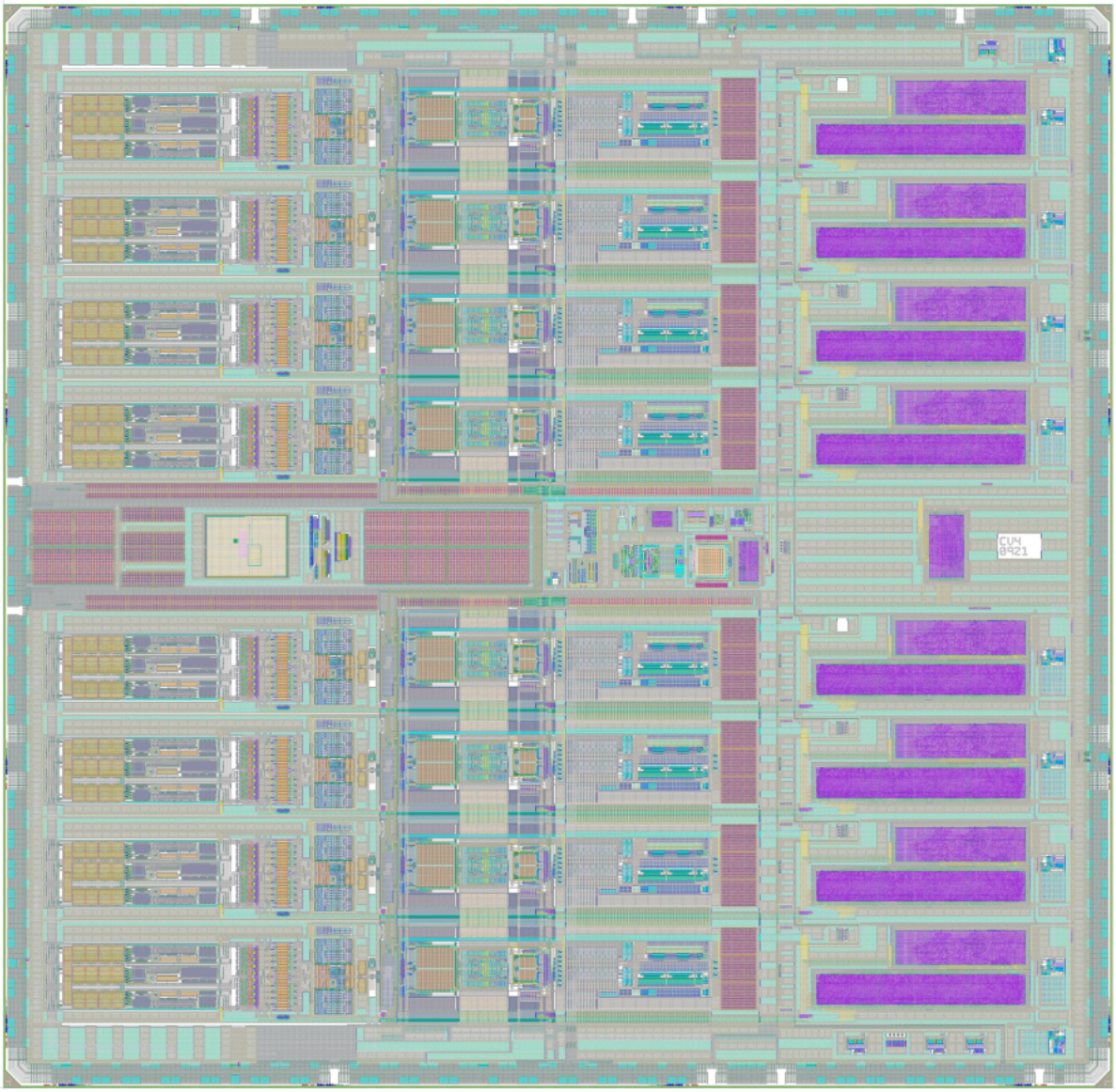

Figure 2: COLUTAV4 layout

3 QFN Packaged Interface

Figure 3 and table 1 highlight the physical interconnections to the COLUTAV4 device when following Section 2 and the recommended wirebonding and packaging engineering drawing (separate document).

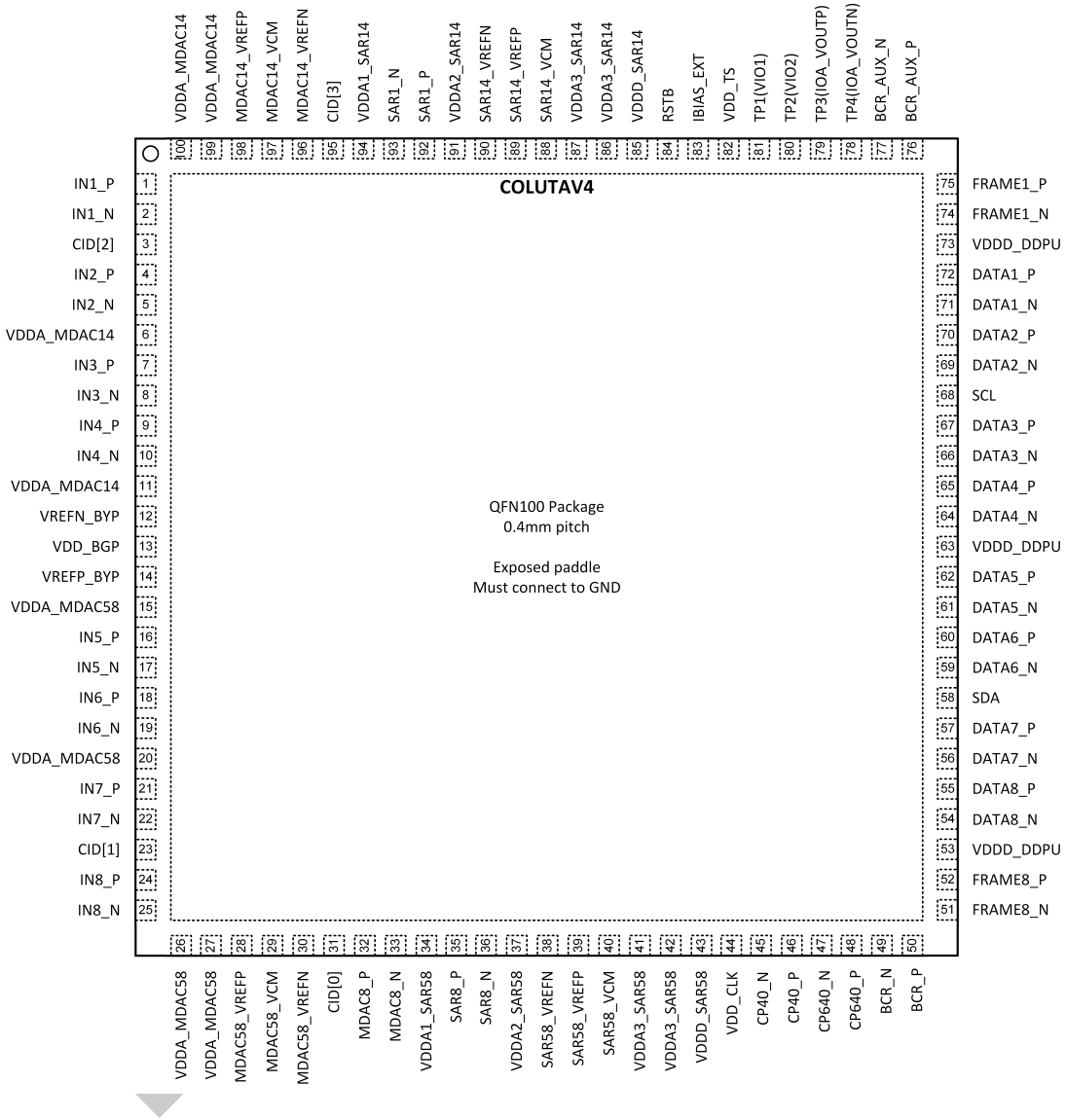

Figure 3: COLUTAV4 pin diagram

Table 1: Pin Mapping

Pin	Name	Direction	Description
1	IN1_P	Analog In	Channel 1 signal input, positive.
2	IN1_N	Analog In	Channel 1 signal input, negative.
3	CID[2]	Digital In	Chip ID, bit 2.
4	IN2_P	Analog In	Channel 2 signal input, positive.
5	IN2_N	Analog In	Channel 2 signal input, negative.
6	VDDA_MDAC14	Power	1.2V analog VDD for MDAC channels 1-4.
7	IN3_P	Analog In	Channel 3 signal input, positive.
8	IN3_N	Analog In	Channel 3 signal input, negative.
9	IN4_P	Analog In	Channel 4 signal input, positive.
10	IN4_N	Analog In	Channel 4 signal input, negative.
11	VDDA_MDAC14	Power	1.2V analog VDD for MDAC channels 1-4.
12	VREFN_BYP	Analog I/O	Bypass for 100mV reference. Provide with external source whose impedance is less than 5 kOhms or daisy-chain with another COLUTAV3 chip, if desired. Use low-ESR, low-ESL bypass capacitors of more than 1μF to ground and VREFP_BYP.
13	VDD_BGP	Power	1.2V analog VDD for on-chip bandgap reference.
14	VREFP_BYP	Analog I/O	Bypass for 1.1V reference. Provide with external source whose impedance is less than 5 kOhms or daisy-chain with another COLUTAV3 chip, if desired. Use low-ESR, low-ESL bypass capacitors of more than 1μF to ground and VREFN_BYP.
15	VDDA_MDAC58	Power	1.2V analog VDD for MDAC channels 5-8.
16	IN5_P	Analog In	Channel 5 signal input, positive.
17	IN5_N	Analog In	Channel 5 signal input, negative.
18	IN6_P	Analog In	Channel 6 signal input, positive.
19	IN6_N	Analog In	Channel 6 signal input, negative.
20	VDDA_MDAC58	Power	1.2V analog VDD for MDAC channels 5-8.
21	IN7_P	Analog In	Channel 7 signal input, positive.
22	IN7_N	Analog In	Channel 7 signal input, negative.

Continued on next page

Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
23	CID[1]	Digital In	Chip ID, bit 1.
24	IN8_P	Analog In	Channel 8 signal input, positive.
25	IN8_N	Analog In	Channel 8 signal input, negative.
26	VDDA_MDAC58	Power	1.2V analog VDD for MDAC channels 5-8.
27	VDDA_MDAC58	Power	1.2V analog VDD for MDAC channels 5-8.
28	MDAC58_VREFP	Analog I/O	MDAC external 1.1V input. Bypass to ground if not used.
29	MDAC58_VCM	Analog I/O	MDAC external 600mV input. Bypass to ground if not used.
30	MDAC58_VREFN	Analog I/O	MDAC external 100mV input. Bypass to ground if not used.
31	CID[0]	Digital In	Chip ID bit 0 (LSB).
32	MDAC8_P	Analog Out	Channel 8 MDAC debug output, positive.
33	MDAC8_N	Analog Out	Channel 8 MDAC debug output, negative.
34	VDDA1_SAR58	Power	1.2V analog VDD for SAR channels 5-8.
35	SAR8_P	Analog Out	Channel 8 SAR debug input, positive.
36	SAR8_N	Analog Out	Channel 8 SAR debug input, negative.
37	VDDA2_SAR58	Power	1.2V analog VDD for SAR channels 5-8.
38	SAR58_VREFN	Analog I/O	SAR external 100mV input. Bypass to ground if not used.
39	SAR58_VREFP	Analog I/O	SAR external 1.1V input. Bypass to ground if not used.
40	SAR58_VCM	Analog I/O	SAR external 600mV input. Bypass to ground if not used.
41	VDDA3_SAR58	Power	1.2V Analog VDD for SAR channels 5-8.
42	VDDA3_SAR58	Power	1.2V Analog VDD for SAR channels 5-8.
43	VDDD_SAR58	Power	1.2V digital VDD for SAR channels 5-8.
44	VDD_CLK	Power	1.2V Analog VDD for clock distribution.
45	CP40_N	Digital In	40MHz sLVDS clock input, negative.
46	CP40_P	Digital In	40MHz sLVDS clock input, positive.
47	CP640_N	Digital In	640MHz sLVDS clock input, negative.

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Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
48	CP640_P	Digital In	640MHz sLVDS clock input, positive.
49	BCR_N	Digital In	BC Reset sLVDS clock input, negative.
50	BCR_P	Digital In	BC Reset sLVDS clock input, positive.
51	FRAME8_N	Digital Out	Channel 8 FRAME sLVDS output, negative.
52	FRAME8_P	Digital Out	Channel 8 FRAME sLVDS output, positive.
53	VDDD_DDPU	Power	1.2V digital VDD for channels 1-8.
54	DATA8_N	Digital Out	DATA8 sLVDS output, negative.
55	DATA8_P	Digital Out	DATA8 sLVDS output, positive.
56	DATA7_N	Digital Out	DATA7 sLVDS output, negative.
57	DATA7_P	Digital Out	DATA7 sLVDS output, positive.
58	SDA	Analog I/O	I^2C slave data, open-drain.
59	DATA6_N	Digital Out	DATA6 sLVDS output, negative.
60	DATA6_P	Digital Out	DATA6 sLVDS output, positive.
61	DATA5_N	Digital Out	DATA5 sLVDS output, negative.
62	DATA5_P	Digital Out	DATA5 sLVDS output, positive.
63	VDDD_DDPU	Power	1.2V digital VDD for channels 1-8.
64	DATA4_N	Digital Out	DATA4 sLVDS output, negative.
65	DATA4_P	Digital Out	DATA4 sLVDS output, positive.
66	DATA3_N	Digital Out	DATA3 sLVDS output, negative.
67	DATA3_P	Digital Out	DATA3 sLVDS output, positive.
68	SCL	Digital In	I^2C slave clock.
69	DATA2_N	Digital Out	DATA2 sLVDS output, negative.
70	DATA2_P	Digital Out	DATA2 sLVDS output, positive.
71	DATA1_N	Digital Out	DATA1 sLVDS output, negative.
72	DATA1_P	Digital Out	DATA1 sLVDS output, positive.
73	VDDD_DDPU	Power	1.2V digital VDD for channels 1-8.
74	FRAME1_N	Digital Out	Channel 1 FRAME sLVDS output, negative.
75	FRAME1_P	Digital Out	Channel 1 FRAME sLVDS output, positive.
76	BCR_AUX_P	Digital In	Auxiliary BC Reset sLVDS clock input, positive.

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Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
76	BCR_AUX_N	Digital In	Auxiliary BC Reset sLVDS clock input, negative.
78	TP4(IOA_VOUTN)	Analog I/O	Testpoint 4.
79	TP3(IOA_VOUTP)	Analog I/O	Testpoint 3.
80	TP2(VIO2)	Analog I/O	Testpoint 2.
81	TP1(VIO1)	Analog I/O	Testpoint 1.
82	VDD_TS	Power	1.2V analog VDD for test structures.
83	IBIAS_EXT	Analog In	External 200μA current input (from 1.2V analog VDD) when not using internal bandgap reference. Otherwise, decouple to ground.
84	RSTB	Digital In	I^2C slave active-low reset.
85	VDDD_SAR14	Power	1.2V digital VDD for SAR channels 1-4.
86	VDDA3_SAR14	Power	1.2V analog VDD for SAR channels 1-4.
87	VDDA3_SAR14	Power	1.2V analog VDD for SAR channels 1-4.
88	SAR14_VCM	Analog I/O	SAR external 600mV input. Bypass to ground if not used.
87	SAR14_VREFP	Analog I/O	SAR external 1.1V input. Bypass to ground if not used.
90	SAR14_VREFN	Analog I/O	SAR external 100mV input. Bypass to ground if not used.
89	VDDA2_SAR14	Power	1.2V analog VDD for SAR channels 1-4.
92	SAR1_P	Analog In	Channel 1 SAR debug input, positive.
93	SAR1_N	Analog In	Channel 1 SAR debug input, negative.
94	VDDA1_SAR14	Power	1.2V analog VDD for SAR channels 1-4.
95	CID[3]	Digital In	Chip ID bit 3 (MSB).
96	MDAC14_VREFN_IN	Analog In	MDAC external 100mV input. Bypass to GND if not used.
97	MDAC14_VCM_IN	Analog In	MDAC external 600mV input. Bypass to GND if not used.
98	MDAC14_VREFP_IN	Analog In	MDAC external 1.100V input. Bypass to GND if not used.
99	VDDA_MDAC14	Power	1.2V analog VDD for MDAC channels 1-4.

Continued on next page

Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
100	VDDA_MDAC14	Power	1.2V analog VDD for MDAC channels 1-4.
Pad	GND	Power	Ground. This must have a low-impedance connection to the circuit ground for good electrical performance and heat dissipation.

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4 Electrical Interface

The COLUTAV4 device must be driven according to the specifications described within this section for optimal performance. All analog inputs are differential and are DC-coupled to the CMOS circuitry within the chip. Electrical interfacing to the COLUTAV4 analog inputs are summarized in table 2.

Temp=entire range, all corners, VDD=1.2V

Specification	**Notes**	**Min**	**Typ**	**Max**	**Units**
C_L Capacitive load	Single-ended value		8		pF
V_{FS} Full-scale swing	Differential			2.0	Volts pk-pk
$V_{FS[U,L]}$ Input range	Single-ended. With respect to ground.	0.1		1.1	Volts
V_{CM} Common-mode input voltage	VDD/2		0.6		Volts

Table 2: Requirements for driving the analog inputs.

5 I²C Control Format

The COLUTAV4 is intended to be used as an I²C slave device. The control structure of the chip features independently addressable write-only bits, where these bits are partitioned on a per-channel basis ("channel slow-control") and a set of general-purpose use bits ("global slow-control"). The on-chip I²C controller addresses uses one-hot encoding to address the slow-control blocks, thus all slow-control bits may either be addressed individually or simultaneously according to table 3. The global slow-control bank contains 24 read-only bits in addition to its write-only bits. The I²C slave controller can independently address up to eight channel slow-control blocks and the global slow-control block.

Address	Destination
8'h01	Channel 1 (MDAC+SAR)
8'h02	Channel 2 (MDAC+SAR)
8'h04	Channel 3 (MDAC+SAR)
8'h08	Channel 4 (MDAC+SAR)
8'h10	Channel 5 (MDAC+SAR)
8'h20	Channel 6 (MDAC+SAR)
8'h40	Channel 7 (MDAC+SAR)
8'h80	Channel 8 (MDAC+SAR)

Table 3: Channel slow-control addressing.

5.1 Channel Slow-Control Control Bits

Tables 4, 5, 6, and 7 detail the assignments of the channel slow-control bits that are identical to every channel. The highest bit position indicates the most-significant bit.

Table 4: Channel-wide slow-control bit mapping.

sc_ch<>	Description
<543>	**CH:DATA_TX Drive Strength** Default: 1'b1
<542>	**CH:FRAME_TX Drive Strength** Default: 1'b1
<541:539>	**CH:DATA_MUX Select** Default: 3'b000 3'b000: Current channel data A 3'b001: Adjacent channel data B 3'b010: CP40_DDPU 3'b011: CP80_DDPU 3'b100: CP640_DDPU 3'b101: BCR_DDPU 3'b110: Current channel data B 3'b111: Current channel FRAME
<538:536>	**Un-used**
<535>	**CH:TP1 Pass-thru** Default: 1'b0
<534>	**CH:DISABLE** Default: 1'b0 1'b0: Channel analog biasing enabled. 1'b1: Channel analog biasing disabled.
<533:531>	**CH:Testpoint Select** Default: 3'h0 3'b000: TP1=MDAC_VREFP; TP2=MDAC_VREFN 3'b001: TP1=GND; TP2=GND 3'b010: TP1=VDD_MDAC; TP2=MDAC_VCM 3'b011: TP1=GND; TP2=GND 3'b100: TP1=VDD_AMP_SAR; TP2=VDD_REF_SAR 3'b101: TP1=GND; TP2=GND 3'b110: TP1=TP1_thru; TP=TP2_thru 3'b111: TP1=25μA sink; TP2=GND
<530:529>	**Un-used**
<528>	**CH:TP2 Pass-thru** Default: 1'b1

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Table 5: Channel MDAC slow-control bit mapping. Applicable only to channels 5-8.

sc_ch<>	Description
<527>	**MDAC:CAL_FORCESR** Default: 1'b0 1'b0: Subrange is not forced in subADC 1'b1: Subrange is forced in subADC
<526:519>	**MDAC:CAL_SRVAL** Default: 8'h00
<518>	**MDAC:CAL_FORCEDAC** Default: 1'b0 1'b0: capDAC is not forced 1'b1: capDAC is forced
<517:510>	**MDAC:CAL_DACP** Default: 8'h00
<509:502>	**MDAC:CAL_DACM** Default: 8'h00
<501:499>	**MDAC:STROBE** Default: 3'b100
<498:496>	**MDAC:AMP_STG2** Default: 3'h2
<495:488>	**MDAC:IDAC** Default: 8'hA8
<487>	**MDAC:CB_M_EN** Default: 1'b1
<486:485>	**MDAC:CB_M_STGTWO** Default: 2'h1
<484:479>	**MDAC:CB_M_IREF** Default: 6'h2B
<478>	**MDAC:CB_M_ONCHIP** Default: 1'b1
<477>	**MDAC:CB_C_EN** Default: 1'b1
<476:475>	**MDAC:CB_C_STGTWO** Default: 2'h0
<474:469>	**MDAC:CB_C_IREF** Default: 6'h29
<468>	**MDAC:CB_C_ONCHIP** Default: 1'b1
<467>	**MDAC:CB_P_EN** Default: 1'b1
<466:465>	**MDAC:CB_P_STGTWO** Default: 2'h2

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Table 5 – *Continued from previous page*

sc_ch<>	Description
<464:459>	**MDAC:CB_P_IREF** Default: 6'h29
<458>	**MDAC:CB_P_ONCHIP** Default: 1'b1
<457>	**MDAC:CLK_EN** Default: 1'b1
<456>	**MDAC:CLK_MDAC_SAMP_EN** Default: 1'b1
<455>	**MDAC:CLK_RESET_EN** Default: 1'b1
<454>	**MDAC:CLK_SUBADC_SAMP_EN** Default: 1'b1
<453>	**MDAC:EN_VOUT2EXT** Default: 1'b0

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Table 6: Channel SAR slow-control bit mapping.

sc<>	Description
<452>	**SAR:EN_RB_VREFN** Default: 1'b1
<451>	**SAR:EN_RB_VCM** Default: 1'b1
<450>	**SAR:EN_RB_VREFP** Default: 1'b1
<449>	**SAR:RB2EXT_VREFN_FStage** Default: 1'b0
<448>	**SAR:RB2EXT_VREFN_CStage** Default: 1'b0
<447>	**SAR:RB2EXT_VCM** Default: 1'b0
<446>	**SAR:RB2EXT_VREFP_FStage** Default: 1'b0
<445>	**SAR:RB2EXT_VREFP_CStage** Default: 1'b0
<444>	**SAR:SHORT_INPUT** Default: 1'b0
<443>	**SAR:DREMDAC_TO_SAR** Default: 1'b1
<442>	**SAR:EXT_TO_SAR** Default: 1'b0
<441>	**SAR:CLK_EN** Default: 1'b1
<440>	**SAR:S_AMP** Default: 1'b1 1'b0: 50% decision cycle 1'b1: 25% decision cycle
<439:432>	**SAR:VREF_PBOOST** Default: 8'h37
<431:424>	**SAR:VREF_NBOOST** Default: 8'h37
<423:416>	**SAR:VREF_MAIN** Default: 8'h37
<415:410>	**SAR:IBIAS_FLOOP** Default: 6'h0D
<409:404>	**SAR:IBIAS_CLOOP** Default: 6'h0D
<403:398>	**SAR:IBIAS_RBCM** Default: 6'h0D

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Table 6 – *Continued from previous page*

sc<>	Description
<397:392>	**SAR:IBIAS_RBP** Default: 6'h0D
<391:386>	**SAR:IBIAS_RBN** Default: 6'h0D
<385:380>	**SAR:IBIAS_PBOOST** Default: 6'h0D
<379:374>	**SAR:IBIAS_NBOOST** Default: 6'h0D
<373:368>	**SAR:IBIAS_MAIN_OP** Default: 6'h0D
<367:348>	**SAR:CAL_REGB** Default: 20'h00000
<347:328>	**SAR:CAL_REGA** Default: 20'h00000
<327>	**SAR:CAL_DIR** Default: 1'b0
<326>	**SAR:CAL_PN_DAC** Default: 1'b0
<325:304>	**SAR:CAL_EN** Default: 22'h000000

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Table 7: Channel DDPU slow-control bit mapping.

sc_ch<>	Description
<303>	**DDPU:INVERT_MDAC0** Default: 1'b0
<302:291>	**DDPU:FEB_ID** Default: 12'h000
<290:274>	**DDPU:MDAC Correction Code 7** Default: 17'b11100000000000000
<273:257>	**DDPU:MDAC Correction Code 6** Default: 17'b11000000000000000
<256:240>	**DDPU:MDAC Correction Code 5** Default: 17'b10100000000000000
<239:223>	**DDPU:MDAC Correction Code 4** Default: 17'b10000000000000000
<222:206>	**DDPU:MDAC Correction Code 3** Default: 17'b01100000000000000
<205:189>	**DDPU:MDAC Correction Code 2** Default: 17'b01000000000000000
<188:172>	**DDPU:MDAC Correction Code 1** Default: 17'b00100000000000000
<171:155>	**DDPU:MDAC Correction Code 0** Default: 17'b00000000000000000
<154:141>	**DDPU:SAR Correction Code 20** Default: 14'b11100000000000
<140:127>	**DDPU:SAR Correction Code 19** Default: 14'b10000000000000
<126:114>	**DDPU:SAR Correction Code 18** Default: 13'b1000000000000
<113:102>	**DDPU:SAR Correction Code 17** Default: 12'b101000000000
<101:91>	**DDPU:SAR Correction Code 16** Default: 11'b11000000000
<90:80>	**DDPU:SAR Correction Code 15** Default: 11'b10000000000
<79:70>	**DDPU:SAR Correction Code 14** Default: 10'b1000000000
<69:60>	**DDPU:SAR Correction Code 13** Default: 10'b1110000000
<59:50>	**DDPU:SAR Correction Code 12** Default: 10'b1000000000
<49:41>	**DDPU:SAR Correction Code 11** Default: 9'b100000000

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Table 7 – *Continued from previous page*

sc_ch<>	Description
<40:33>	**DDPU:SAR Correction Code 10** Default: 8'b10000000
<32:26>	**DDPU:SAR Correction Code 9** Default: 7'b1100000
<25:19>	**DDPU:SAR Correction Code 8** Default: 7'b1000000
<18:13>	**DDPU:SAR Correction Code 7** Default: 6'b101000
<12:8>	**DDPU:SAR Correction Code 6** Default: 5'b11000
<7>	**DDPU:Serializer Test Mode** Default: 1'b0 1'b0: Normal data 1'b1: Test pattern
<6>	**DDPU:Correction Enable** Default: 1'b1
<5>	**DDPU:Output Mode** Default: 1'b0 1'b0: Normal 16-bit mode 1'b1: Debug 32-bit mode
<4>	**DDPU:Data Flavor** Default: 1'b0 1'b0: MDAC mode 1'b1: Misc data mode
<3:0>	**DDPU:LPGBT Phase** Default: 4'h0

5.2 Global Slow-Control Bits

The global slow-control bits (table 9) are allocated to shared resources including the clock distribution, on-chip bandgap, and test structure blocks. There exists 24 read-only bits.

Table 8: Global read-only bit mapping.

`read_global<>`	**Description**
<23> *XS mode*	**XS_gatestat** Active-low counting status in XS mode.
<22> *XS mode*	**XS_overflow** Active-high overflow flag in XS mode.
<21:0> *XS mode*	**XS_count** Count value in XS mode.
<23:12> *MADC mode*	**SAMP1** First sample from MADC.
<11:0> *MADC mode*	**SAMP2** Second sample from MADC.

Table 9: Global control bit mapping.

`sc_global<>`	**Description**
<127>	**TS:INT_EN_VREFSENSE** Default: `1'b0` `1'b0`: Disable VREF sensing `1'b1`: Enable VREF sensing
<126>	**TS:INT_EN_CORNER** Default: `1'b0` `1'b0`: Disable corner sensing `1'b1`: Enable corner sensing

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Table 9 – *Continued from previous page*

sc_global<>	Description
<125:124>	**TS:INT_SEL** Default: 3'b000 3'b000: NBIAS50u with shunt 3'b001: Half-VDD 3'b010: VREFP with shunt 3'b011: VCM with shunt 3'b100: VREFN with shunt 3'b101: Half-VDD 3'b110: NMOS corner 3'b111: PMOS corner
<122:120>	**TS:TP_SEL** Default: 3'b000 3'b000: (TP1=GND, TP2=GND) or ch1 3'b001: (TP1=BGP_50u, TP2=BGP_VCM) or ch2 3'b010: (TP1=GND, TP2=GND) or ch3 3'b011: (TP1=VDDD_CLK, TP2=VDD_BGP) or ch4 3'b100: (TP1=GND, TP2=GND) or ch5 3'b101: (TP1=VDDD_DDPU, TP2=GND) or ch6 3'b110: (TP1=GND, TP2=GND) or ch7 3'b111: (TP1=GND, TP2=GND) or ch8
<119>	**TS:XS_VBOT_GND** Default: 1'b0 1'b0: High-Z 1'b1: Grounded
<118>	**TS:XS_LOWGAIN** Default: 1'b0 1'b0: x10 gain 1'b1: x2 gain
<117:110>	**TS:DI_BIAS** Default: 8'd128

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Table 9 – *Continued from previous page*

sc_global<>	Description
<109:106>	**TS:DI_SEL** Default: 4'b0000 4'b0000: TP1=NLOGIC1; TP2=NIO1 4'b0001: TP1=NLOGIC4; TP2=NIO4 4'b0010: TP1=NLOGIC1_ENC; TP2=NIO1_ENC 4'b0011: TP1=NLOGIC4_ENC; TP2=NIO4_ENC 4'b0100: TP1=PLOGIC1; TP2=PIO1 4'b0101: TP1=PLOGIC4; TP2=PIO4 4'b0110: TP1=PLOGIC1_ENC; TP2=PIO1_ENC 4'b0111: TP1=PLOGIC4_ENC; TP2=PIO4_ENC 4'b1000: TP1=NLOGIC4-TEMP; TP2=PLOGIC4-TEMP 4'b1001: TP1=NLOGIC4_ENC-TEMP; TP2=PLOGIC4_ENC-TEMP 4'b1010: TP1=NIO4-TEMP; TP2=PIO4-TEMP 4'b1011: TP1=NIO4_ENC-TEMP; TP2=PIO4_ENC-TEMP 4'b1100: TP1=VBIASP; TP2=VBIASN 4'b1101: TP1=IBIASP; TP2=IBIASN 4'b1110: TP1=VBIASP; TP2=VBIASP 4'b1111: TP1=VBIASN; TP2=VBIASN
<105>	**TS:XS_RSTMODE** Default: 1'b1 1'b0: Auto 1'b1: RSTMAN
<104>	**TS:XS_RSTMAN** Default: 1'b0 1'b0: Open 1'b1: Closed (reset)
<103:101>	**TS:XS_SEUSEL** Default: 3'b000 3'b000: Open 3'b001: Short 3'b010: APS1 3'b011: APS2 3'b100: MOM1 3'b101: MOM2 3'b110: MIM1 3'b111: MIM2

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Table 9 – *Continued from previous page*

sc_global<>	Description
<100:99>	**TS:IOA_MUX** Default: 2'b00 2'b00: Dosimeter 2'b01: XS 2'b10: Internal Sense 2'b11: Open
<98>	**TS:IOA_TP2IOA** Default: 1'b0 1'b0: Open 1'b1: Closed (TP12=IOA)
<97>	**TS:IOA_FEENABLE** Default: 1'b1
<96>	**TS:IOA_SWIN** Default: 1'b0 1'b0: Front-end 1'b1: Back-end
<95:92>	**TS:IOA_FEG** Default: 4'h0 4'h0: x(16/16)+1 4'h1: x(16/15)+1 4'h2: x(16/14)+1 4'h3: x(16/13)+1 4'h4: x(16/12)+1 4'h5: x(16/11)+1 4'h6: x(16/10)+1 4'h7: x(16/9)+1 4'h8: x(16/8)+1 4'h9: x(16/7)+1 4'hA: x(16/6)+1 4'hB: x(16/5)+1 4'hC: x(16/4)+1 4'hD: x(16/3)+1 4'hE: x(16/2)+1 4'hF: x(16/1)+1
<91>	**TS:IOA_FEUG** Default: 1'b0 1'b0: Non-unity gain 1'b1: Unity gain
<90>	**TS:IOA_BEENABLE** Default: 1'b1

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Table 9 – *Continued from previous page*

sc_global<>	Description
<89:86>	**TS:IOA_CAP** Default: 4'h8
<85:82>	**TS:IOA_BEG** Default: 4'h0 4'h0: x16/1 4'h1: x15/1 4'h2: x14/1 4'h3: x13/1 4'h4: x12/1 4'h5: x11/1 4'h6: x10/1 4'h7: x9/1 4'h8: x8/1 4'h9: x7/1 4'hA: x6/1 4'hB: x5/1 4'hC: x4/1 4'hD: x3/1 4'hE: x2/1 4'hF: x1/1
<81:78>	**TS:TP12_MUX** Default: 4'b0000 4'b0000: IOA FE 4'b0001: IOA BE 4'b0010: Channel TP 4'b0011: Global TP 4'b0100: TP1=XS_nCTRST; TP2=XS_CTGateStat 4'b0101: TP1=XS_VBOT; TP2=XS_VDIFF 4'b0110: TP1=XS_VBOT; TP2=GND 4'b0111: TP1=XS_VBOT; TP2=XS_CMP 4'b1000: TP1=XS_VBOT; TP2=XS_SEUINC 4'b1001: TP1=XS_VBOT; TP2=XS_LR 4'b1010: TP1=GND; TP2=GND 4'b1011: TP1=XS_VDIFF; TP2=GND 4'b1100: TP1=GND; TP2=XS_CMP 4'b1101: TP1=GND; TP2=XS_SEUINC 4'b1110: TP1=GND; TP2=XS_LR 4'b1111: TP1=XS_SEUINC; TP2=XS_LR
<77>	**TS:DISABLE** Default: 1'b0

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Table 9 – *Continued from previous page*

sc_global<>	Description
<76>	**TS:XS_nPSRST** Default: 1'b0 1'b0: Pre-scaler reset 1'b1: Active
<75>	**TS:XS_nCTRST** Default: 1'b0 1'b0: Counter reset 1'b1: Active
<74:72>	**TS:XS_GTLEN** Default: 3'b000 3'b000: 0.8388 s 3'b001: 1.6777 s 3'b010: 3.3554 s 3'b011: 6.7109 s 3'b100: 13.4218 s 3'b101: 26.8435 s 3'b110: 53.6871 s 3'b111: 107.3742 s
<71>	**TS:XS_GTMAN** Default: 1'b1 1'b0: Armed 1'b1: Hold Count
<70>	**TS:XS_GTMODE** Default: 1'b0 1'b0: Internal 1'b1: GTMAN
<69:68>	**TS:XS_LR_PS** Default: 2'b00 2'b00: 156.25 kHz 2'b01: 312.5 kHz 2'b10: 625 kHz 2'b11: 1.25 MHz
<67:62>	**TS:XS_VT_HIGH** Default: 6'h20
<61:56>	**TS:XS_VT_LOW** Default: 6'h20

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Table 9 – *Continued from previous page*

sc_global<>	Description
<55:54>	**TS:XS_BE_SEL** Default: 2'b00 2'b00: analog 2'b01: 1DFF 2'b10: DFF TMR not spaced 2'b11: DFF TMR spaced
<53>	**TS:XS_DFF_POL** Default: 1'b0 1'b0: Load 0 1'b1: Load 1
<52>	**TS:XS_DIFFAMP_GAINSEL** Default: 1'b0 1'b0: unity 1'b1: x4 gain
<51>	**TS:DOUT_SEL** Default: 1'b0 1'b0: XS Measurement 1'b1: Slow-ADC
<50>	**TS:MADC_nRST** Default: 1'b1 1'b0: Reset 1'b1: Active
<49:48>	**TS:MADC_CLKPS** Default: 2'b00 2'b00: divide-by-1 2'b01: divide-by-4 2'b10: divide-by-8 2'b11: divide-by-16
<47:34>	Not used.
<33:29>	**BGP:RDAC_CODE_VCM** Default: 5'd16
<28>	**BGP:EN_VCM** Default: 1'b1 1'b0: High-Z 1'b1: Enabled
<27:23>	**BGP:RDAC_CODE_VREFP** Default: 5'd13
<22>	**BGP:EN_VREFP** Default: 1'b1 1'b0: High-Z 1'b1: Enabled

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Table 9 – *Continued from previous page*

sc_global<>	Description
<21>	**BGP:EN_VREFN** Default: 1'b1 1'b0: High-Z 1'b1: Enabled
<20:16>	**BGP:RDAC_CODE_VREFN** Default: 5'd13
<15>	**BGP:SEL_IBIAS** Default: 1'b1 1'b0: IBIAS_EXT 1'b1: BGP
<14>	**BGP:EXT_START** Default: 1'b0 1'b0: Normal operation 1'b1: External stimulus Avoid operating at 1'b1 for a prolonged period of time.
<13:11>	**BGP:TRIM_UP** Default: 3'b000
<10:8>	**BGP:TRIM_DOWN** Default: 3'b000
<7:5>	Not used.
<4>	**CLK:INV_640** Default: 1'b0
<3:1>	**CLK:DELAY_640** Default: 3'b000
<0>	**CLK:AUX_BCR** Default: 1'b1 1'b0: Primary BCR 1'b1: Auxiliary BCR

6 Data Output Format

The COLUTAV4 has an output bandwidth of ten 640Mbps serial lanes using sLVDS differential signaling voltage levels and are all intended for a direct and seamless electrical interface to the lpGBT [2]. In all cases, bits are ordered from <15> (MSB) to <0> (LSB).

6.1 FRAME Output

Both FRAME outputs on channels 1 and 8 are of fixed data structure with a data length of 16 bits (1 word). The bit ordering of the FRAME data output is shown in table 10. Two frame outputs exist in the case of data bifurcation to the lpGBT, therefore only sc_ch<542> control the TX drive strength of the respective FRAME output. Channels 2-7 sc_ch<542> are internally un-connected.

The FRAME signal is comprised of two pieces of information: **FRAME:FIRST** and **FRAME:BCNumber** and is reliant on the state of the bunch-crossing reset (BC reset) signal. BC reset is asserted by providing a differential logic 1 to the sLVDS inputs of BCR_P and BCR_N. It is de-asserted by providing a differential logic 0. During BC reset, **FRAME:FIRST** is asserted to 1'b1 and **FRAME:BCNumber** is 5'b00000. Once BC reset is de-asserted, **FRAME:FIRST** is de-asserted and **FRAME:BCNumber** increments by one. The counter counts upward every ADC sample and wraps around continuously, all the while **FRAME:FIRST** is kept to 1'b0 until BC reset is asserted again. The FRAME word and DATA words are aligned bit-wise and therefore the FRAME signal is used to modulo-32 timestamp each ADC sample in synchronization to BC reset.

Table 10: FRAME output bit mapping.

FRAME<>	**Description**
<15>	1'b1
<14>	1'b0
<13>	**FRAME:FIRST** 1'b0: Non-first sample 1'b1: BC Reset is asserted
<12:8>	**FRAME:BCNumber** Bunch-crossing counter
<7:0>	8'h00

6.2 Physical-to-Logical Mapping

The eight physical DATA output channels are individually configurable via slow-control sc_ch<541:539> to different logical channels of the ADC. Three canonical arrangements of channel-to-data exist: normal, even calibration, and odd calibration. These are summarized in table 11. Calibration modes require double the bandwidth for each logical channel to allow for offline calibration of internal circuitry. Additionally, each DATA output has a test pattern that takes precedence to the channel data output and is asserted by setting sc_ch<7> of the respective logical channel. The test pattern bit ordering is shown in table 12.

Output Mode sc_ch<541:539>	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7	DATA8
Normal	Ch. 1A 3'b000	Ch. 2A 3'b000	Ch. 3A 3'b000	Ch. 4A 3'b000	Ch. 5A 3'b000	Ch. 6A 3'b000	Ch. 7A 3'b000	Ch. 8A 3'b000
Even Calibration	Ch. 2B 3'b001	Ch. 2A 3'b000	Ch. 4B 3'b001	Ch. 4A 3'b000	Ch. 6B 3'b001	Ch. 6A 3'b000	Ch. 8B 3'b001	Ch. 8A 3'b000
Odd Calibration	Ch. 1A 3'b000	Ch. 1B 3'b001	Ch. 3A 3'b000	Ch. 3B 3'b001	Ch. 5A 3'b000	Ch. 5B 3'b001	Ch. 7A 3'b000	Ch. 7B 3'b001

Table 11: Data output modes. Columns are physical channels. Rows are canonical output modes. Cells are the corresponding logical channel mapping and sc_ch<541:539> setting.

Table 12: DATA output test pattern bit mapping.

DATA<>	Description
<15:12>	4'b1010
<11:8>	**DATA_SERTEST:CID** Same as Chip ID inputs from the pinout.
<7:5>	**DATA_SERTEST:CHN** Channel number in binary numbering from 3'b000 to 3'b111
<4:0>	If the logical output is type A: 5'b01001 If the logical output is type B: 5'b01010

6.3 Normal Data Mode (sc_ch<7:4> = 4'b0100)

Normal data mode is a direct one-to-one assignment for each channel with a data length of 1 word per lane. Only logical A channels are brought out. The bit ordering of the normal data output per channel is shown in table 13. sc_ch<7:4> must be set to 4'b0100. sc_ch<543> are equally mapped one-to-one to the DATA TX drive strength control of that output.

Table 13: Normal mode output bit mapping.

DATA<>	Description
<15>	**DATA_NORM:OVERFLOW** 1'b0: ADC normal range 1'b1: ADC overflow
<14:0>	**DATA_NORM:ADC_COUNT** ADC binary output

6.4 AUX1 Data Mode (sc_ch<7:4> = 4'b0001)

The physical-logical mapping is the same to that of normal data mode. Only logical A channels are brought out. sc_ch<7:4> must be set to 4'b0001. Table 14 show the bit definition of the output for each channel.

Table 14: AUX1 output bit mapping.

DATA<>	Description
<15:14>	2'b11
<13>	Channels 1-6: 1'b0 Channel 7: **CLK:BE_TEST_80** Channel 8: **CLK:BE_TEST_40**
<12>	Channels 1-6: 1'b0 Channel 7: **CLK:AE_TEST_80** Channel 8: **CLK:AE_TEST_40**
<11:0>	**FEB_ID** From sc_ch<302:291>

Note that in this mode, the contents of channel control signals sc_ch<302:291> are brought out in DATA<11:0>. That is, each channel has a 12 bit slow-control allocation for setting the value of FEB_ID. The value set on the slow-control is registered at the rate of the data converter (40MSPS) by the serializer and transmitted out at the interval of each word.

6.5 AUX2 Data Mode (sc_ch<7:4> = 4'b0011)

The physical-logical mapping is the same to that of normal data mode. Only logical A channels are brought out. sc_ch<7:4> must be set to 4'b0011. Table 15 show the bit definition of the output for each channel.

Table 15: AUX2 output bit mapping.

DATA<>	Description
<15:0>	Channel 1: `16'h8000` Channel 2: `16'h7FFF` Channel 3: `16'h8000` Channel 4: {**MADC<11:0>**, 2'b00, 2'b11} Channel 5: **XS_COUNT<15:0>** Channel 6: {**XS_gatestat**, **XS_overflow**, **XS_count<21:16>**, `4'h0`, `4'hF`} Channel 7: `16'h7FFF` Channel 8: `16'h8000`

6.6 Calibration Data Mode (`sc_ch<7:4>` = 4'b0010)

Both A and B logical outputs of a single channel are mapped to two physical output channels to facilitate a bandwidth of 32 bits per sample per channel. In even calibration mode, even channels are brought out one-to-one while data stream B takes the odd data outputs. In odd calibration mode, odd channels are brought out one-to-one while data stream B takes the even data outputs. `sc_ch<7:4>` must be set to `4'b0010`. Table 16 and 17 show the bit definition of A and B logical outputs.

Table 16: Calibration output bit mapping, logical output A.

DATA<>	Description
<15:14>	`2'b11`
<13>	**DATA_A_MDAC:FLAG** MDAC flag
<12>	**DATA_A_MDAC:VALID** MDAC valid
<11:4>	**DATA_A_MDAC:MDAC** MDAC one-hot raw bits
<3:0>	**DATA_A_MDAC:SAR<19:16>** SAR raw data

Table 17: Calibration output bit mapping, logical output B.

DATA<>	Description
<15:0>	**DATA_B:SAR<15:0>** SAR raw data

References

[1] ATLAS Collaboration, "Technical Design Report for the Phase-II Upgrade of the ATLAS LAr Calorimeter," CERN, Geneva, Tech. Rep. CERN-LHCC-2017-018. ATLAS-TDR-027, Sep 2017. [Online]. Available: https://cds.cern.ch/record/2285582

[2] "lpGBT," https://lpgbt.web.cern.ch/lpgbt/.