COLUTAV3

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Revision History

Revision	Date	Author(s)	Description
0.0	August 28, 2019	RX	Created

Contents

1 Description

The COLUTAV3 device is an 8-channel, precision analog-to-digital converter (ADC) intended for instrumentation readout in radiation-prone areas with an emphasis on mitigating single-event effects. Each channel is intended for operation at 40MSPS and provide $\geq$11 ENOB SNDR. Two design approaches, four of each, are implemented for testing and evaluation: a dynamic range enhancer (DRE) or a multiplying digital-to-analog converter (MDAC), both coupled to an identical successive approximation register (SAR) ADC back-end. The chip is designed in TSMC's 65nm LP 1-poly 6-metal CMOS process.

This device is currently intended for use in the HL-LHC LAr Calorimeter Phase-II upgrade [1].

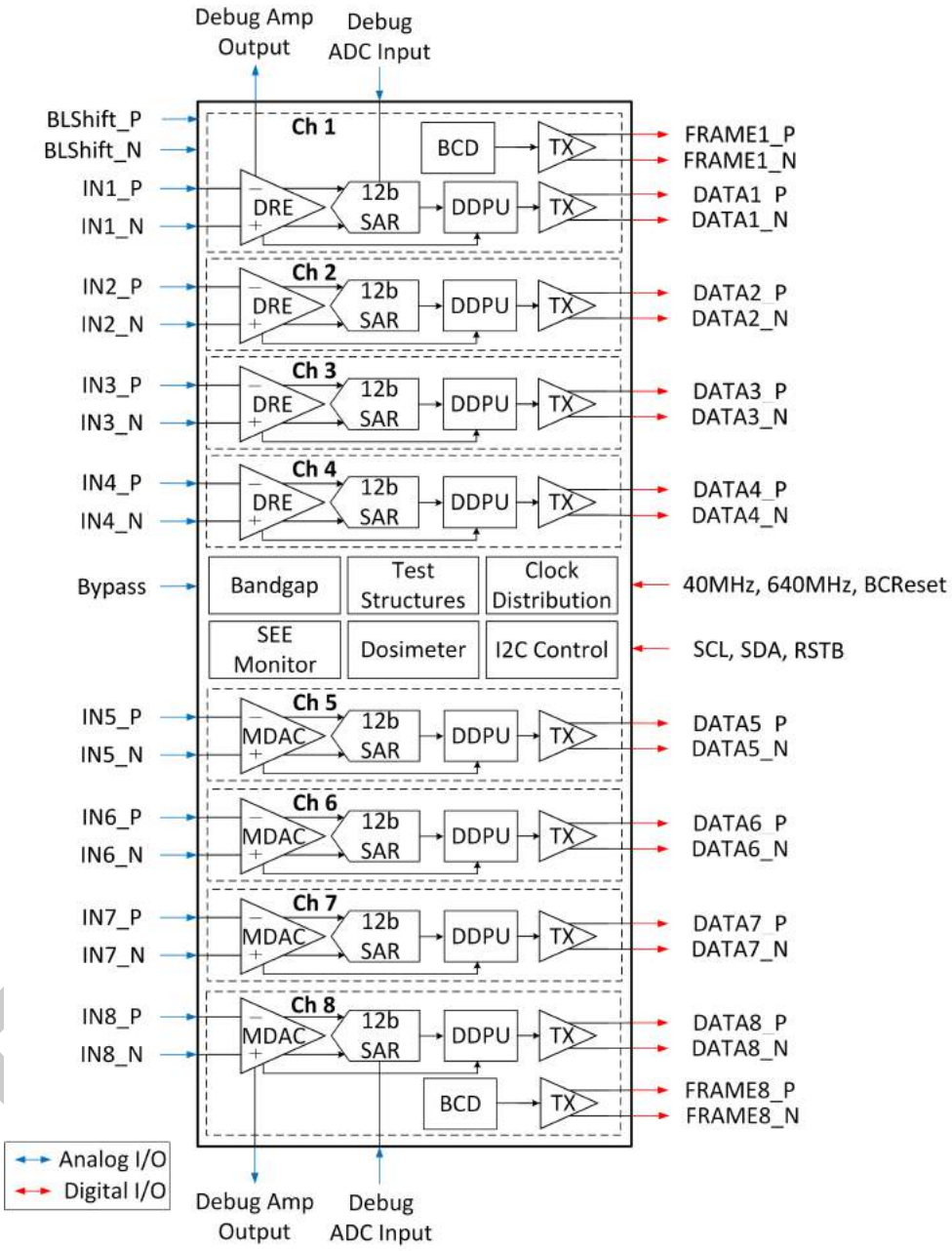

Figure 1: COLUTAV3 functional block diagram

2 Chip Die Information

Figure 2 and 3 show the CAD-drawn layout of the COLUTAV3. The chip measures 5 mm x 5 mm. Wirebonding pads exist along the perimeter of the chip; most analog signals are to be double-bonded and many ground down-bonds are interspersed between I/O pads. Wirebonding should be done using ball-and-wedge bonding with 1 mil diameter gold wire.

The COLUTAV3 chip die is currently only approved to be packaged in a 100-pin, 0.4mm pitch, and with exposed paddle quad-flat no-lead (QFN) open-molded plastic package (OMPP).

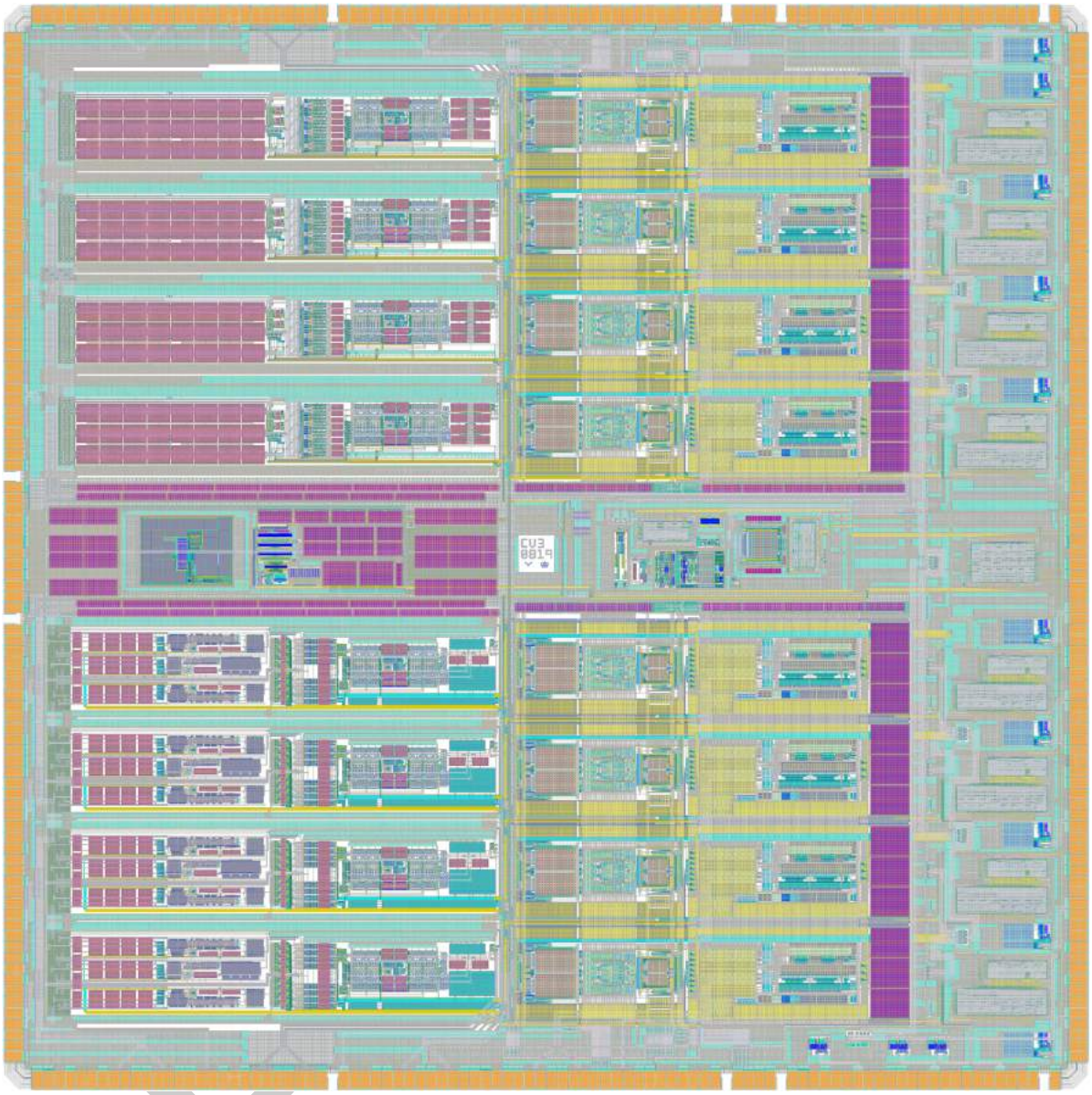

Figure 2: COLUTAV3 CAD-drawn layout. Dimensions measure 5 mm x 5 mm. The orange pattern indicate wirebonding pads. An identifying mark “CV3 0819” exists near the center for purpose of chip identification and alignment (right side up).

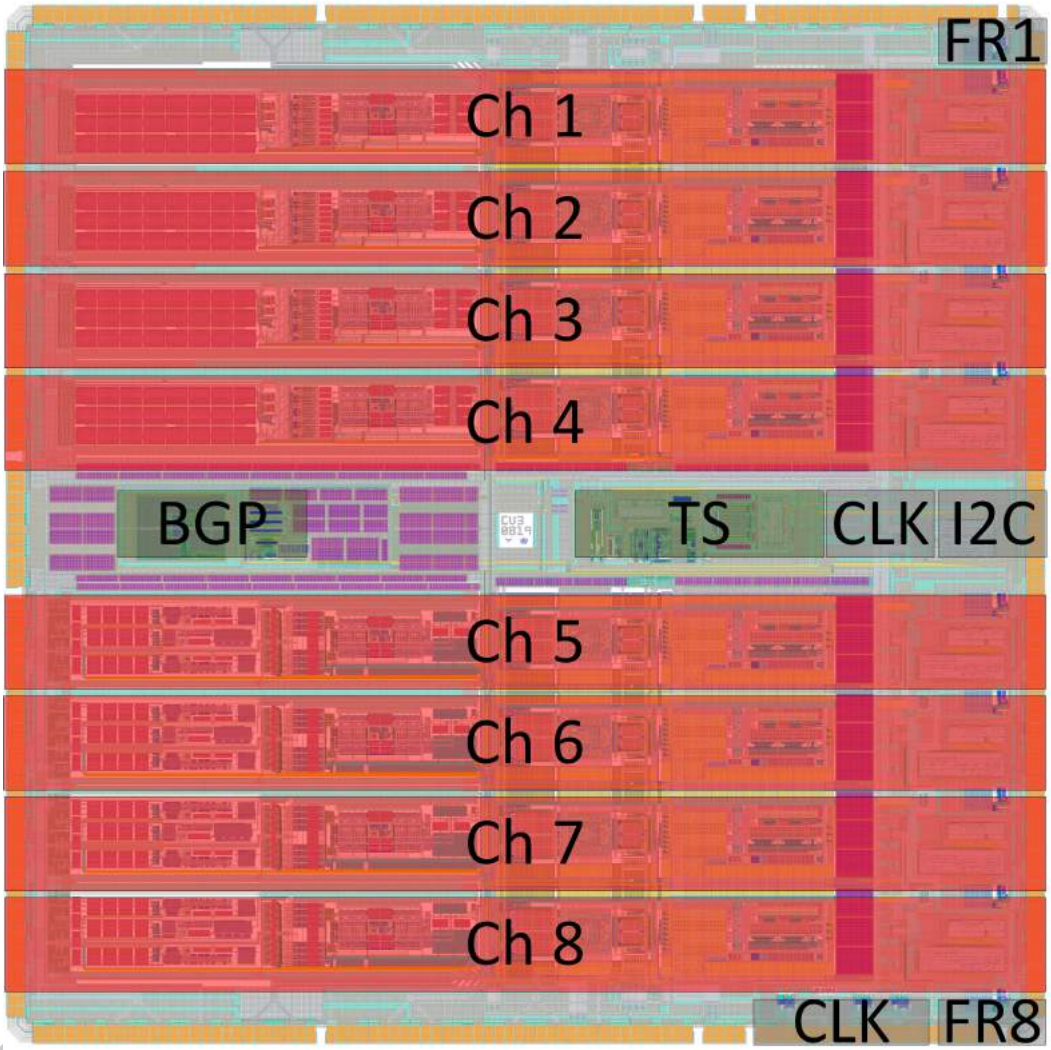

Figure 3: COLUTAV3 CAD-drawn layout, annotated. A DRE/MDAC, SAR, DDPU, channel-level slow-control, sLVDS transmitter, and channel-level DC bias and clock distribution exist within each channel in the red shaded regions. FR1 and FR8 are FRAME1 and FRAME8 transmitters, respectively. Chip-level clock distrbution are in the gray-shaded regions labeled “CLK.” Chip-level slow-control is done in the gray-shaded region labeled “I2C.” Chip-level biasing is done in the green-shaded region labeled “BGP.” Finally, test structures including a dosimeter, a SEE monitor, and a monitoring ADC are located in the green-shaded region labeled “TS.” Bypass capacitors for power and on-chip references exist everywhere else.

3 Packaged Interface

Figure 4 and table 1 highlight the physical interconnections to the COLUTAV3 device when following Section 2 and the recommended wirebonding and packaging engineering drawing (separate document).

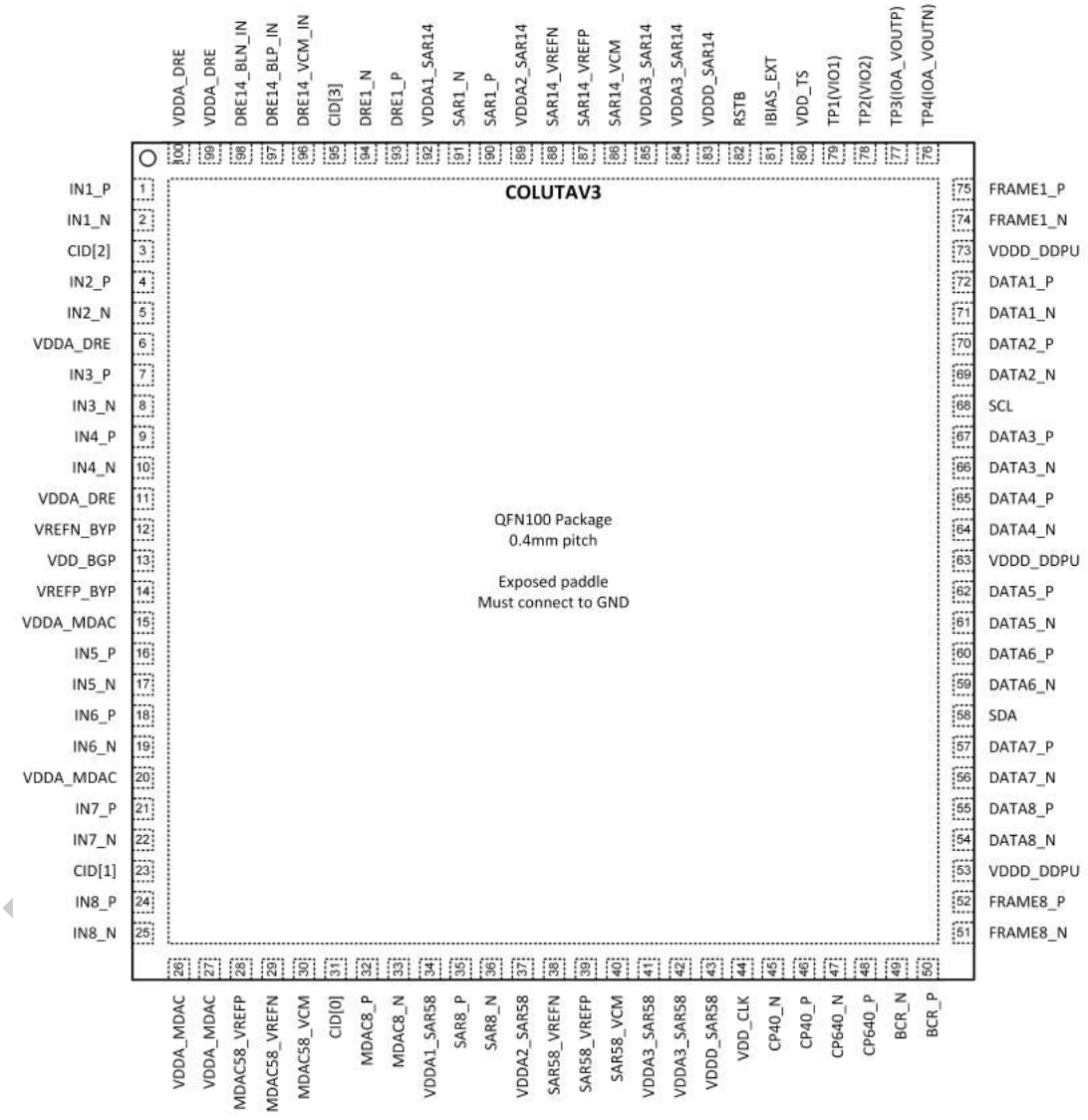

Figure 4: COLUTAV3 pin diagram

Table 1: Pin Mapping

Pin	Name	Direction	Description
1	IN1_P	Analog In	Channel 1 signal input, positive.
2	IN1_N	Analog In	Channel 1 signal input, negative.
3	CID[2]	Digital In	Chip ID, bit 2.
4	IN2_P	Analog In	Channel 2 signal input, positive.
5	IN2_N	Analog In	Channel 2 signal input, negative.
6	VDDA_DRE	Power	1.2V analog VDD for DRE channels 1-4.
7	IN3_P	Analog In	Channel 3 signal input, positive.
8	IN3_N	Analog In	Channel 3 signal input, negative.
9	IN4_P	Analog In	Channel 4 signal input, positive.
10	IN4_N	Analog In	Channel 4 signal input, negative.
11	VDDA_DRE	Power	1.2V analog VDD for DRE channels 1-4.
12	VREFN_BYP	Analog I/O	Bypass for 100mV reference. Provide with external source whose impedance is less than 5 kOhms or daisy-chain with another COLUTAV3 chip, if desired. Use low-ESR, low-ESL bypass capacitors of more than 1μF to ground and VREFP_BYP.
13	VDD_BGP	Power	1.2V analog VDD for on-chip bandgap reference.
14	VREFP_BYP	Analog I/O	Bypass for 1.1V reference. Provide with external source whose impedance is less than 5 kOhms or daisy-chain with another COLUTAV3 chip, if desired. Use low-ESR, low-ESL bypass capacitors of more than 1μF to ground and VREFN_BYP.
15	VDDA_MDAC	Power	1.2V analog VDD for MDAC channels 5-8.
16	IN5_P	Analog In	Channel 5 signal input, positive.
17	IN5_N	Analog In	Channel 5 signal input, negative.
18	IN6_P	Analog In	Channel 6 signal input, positive.
19	IN6_N	Analog In	Channel 6 signal input, negative.
20	VDDA_MDAC	Power	1.2V analog VDD for MDAC channels 5-8.
21	IN7_P	Analog In	Channel 7 signal input, positive.
22	IN7_N	Analog In	Channel 7 signal input, negative.

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Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
23	CID[1]	Digital In	Chip ID, bit 1.
24	IN8_P	Analog In	Channel 8 signal input, positive.
25	IN8_N	Analog In	Channel 8 signal input, negative.
26	VDDA_MDAC	Power	1.2V analog VDD for MDAC channels 5-8.
27	VDDA_MDAC	Power	1.2V analog VDD for MDAC channels 5-8.
28	MDAC58_VREFP	Analog I/O	MDAC external 1.1V input. Bypass to ground if not used.
29	MDAC58_VREFN	Analog I/O	MDAC external 100mV input. Bypass to ground if not used.
30	MDAC58_VCM	Analog I/O	MDAC external 600mV input. Bypass to ground if not used.
31	CID[0]	Digital In	Chip ID bit 0 (LSB).
32	MDAC8_P	Analog Out	Channel 8 MDAC debug output, positive.
33	MDAC8_N	Analog Out	Channel 8 MDAC debug output, negative.
34	VDDA1_SAR58	Power	1.2V analog VDD for SAR channels 5-8.
35	SAR8_P	Analog Out	Channel 8 SAR debug input, positive.
36	SAR8_N	Analog Out	Channel 8 SAR debug input, negative.
37	VDDA2_SAR58	Power	1.2V analog VDD for SAR channels 5-8.
38	SAR58_VREFN	Analog I/O	SAR external 100mV input. Bypass to ground if not used.
39	SAR58_VREFP	Analog I/O	SAR external 1.1V input. Bypass to ground if not used.
40	SAR58_VCM	Analog I/O	SAR external 600mV input. Bypass to ground if not used.
41	VDDA3_SAR58	Power	1.2V Analog VDD for SAR channels 5-8.
42	VDDA3_SAR58	Power	1.2V Analog VDD for SAR channels 5-8.
43	VDDD_SAR58	Power	1.2V digital VDD for SAR channels 5-8.
44	VDD_CLK	Power	1.2V Analog VDD for clock distribution.
45	CP40_N	Digital In	40MHz sLVDS clock input, negative.
46	CP40_P	Digital In	40MHz sLVDS clock input, positive.
47	CP640_N	Digital In	640MHz sLVDS clock input, negative.

Continued on next page

Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
48	CP640_P	Digital In	640MHz sLVDS clock input, positive.
49	BCR_N	Digital In	BC Reset sLVDS clock input, negative.
50	BCR_P	Digital In	BC Reset sLVDS clock input, positive.
51	FRAME8_N	Digital Out	Channel 8 FRAME sLVDS output, negative.
52	FRAME8_P	Digital Out	Channel 8 FRAME sLVDS output, positive.
53	VDDD_DDPU	Power	1.2V digital VDD for channels 1-8.
54	DATA8_N	Digital Out	DATA8 sLVDS output, negative.
55	DATA8_P	Digital Out	DATA8 sLVDS output, positive.
56	DATA7_N	Digital Out	DATA7 sLVDS output, negative.
57	DATA7_P	Digital Out	DATA7 sLVDS output, positive.
58	SDA	Analog I/O	I^2C slave data, open-drain.
59	DATA6_N	Digital Out	DATA6 sLVDS output, negative.
60	DATA6_P	Digital Out	DATA6 sLVDS output, positive.
61	DATA5_N	Digital Out	DATA5 sLVDS output, negative.
62	DATA5_P	Digital Out	DATA5 sLVDS output, positive.
63	VDDD_DDPU	Power	1.2V digital VDD for channels 1-8.
64	DATA4_N	Digital Out	DATA4 sLVDS output, negative.
65	DATA4_P	Digital Out	DATA4 sLVDS output, positive.
66	DATA3_N	Digital Out	DATA3 sLVDS output, negative.
67	DATA3_P	Digital Out	DATA3 sLVDS output, positive.
68	SCL	Digital In	I^2C slave clock.
69	DATA2_N	Digital Out	DATA2 sLVDS output, negative.
70	DATA2_P	Digital Out	DATA2 sLVDS output, positive.
71	DATA1_N	Digital Out	DATA1 sLVDS output, negative.
72	DATA1_P	Digital Out	DATA1 sLVDS output, positive.
73	VDDD_DDPU	Power	1.2V digital VDD for channels 1-8.
74	FRAME1_N	Digital Out	Channel 1 FRAME sLVDS output, negative.
75	FRAME1_P	Digital Out	Channel 1 FRAME sLVDS output, positive.
76	TP4(IOA_VOUTN)	Analog I/O	Testpoint 4.

Continued on next page

Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
77	TP3(IOA_VOUTP)	Analog I/O	Testpoint 3.
78	TP2(VIO2)	Analog I/O	Testpoint 2.
79	TP1(VIO1)	Analog I/O	Testpoint 1.
80	VDD_TS	Power	1.2V analog VDD for test structures.
81	IBIAS_EXT	Analog In	External 200μA current input (from 1.2V analog VDD) when not using internal bandgap reference. Otherwise, decouple to ground.
82	RSTB	Digital In	I^2C slave active-low reset.
83	VDDD_SAR14	Power	1.2V digital VDD for SAR channels 1-4.
84	VDDA3_SAR14	Power	1.2V analog VDD for SAR channels 1-4.
85	VDDA3_SAR14	Power	1.2V analog VDD for SAR channels 1-4.
86	SAR14_VCM	Analog I/O	SAR external 600mV input. Bypass to ground if not used.
87	SAR14_VREFP	Analog I/O	SAR external 1.1V input. Bypass to ground if not used.
88	SAR14_VREFN	Analog I/O	SAR external 100mV input. Bypass to ground if not used.
89	VDDA2_SAR14	Power	1.2V analog VDD for SAR channels 1-4.
90	SAR1_P	Analog In	Channel 1 SAR debug input, positive.
91	SAR1_N	Analog In	Channel 1 SAR debug input, negative.
92	VDDA1_SAR14	Power	1.2V analog VDD for SAR channels 1-4.
93	DRE1_P	Analog Out	Channel 1 DRE debug output, positive.
94	DRE1_N	Analog Out	Channel 1 DRE debug output, negative.
95	CID[3]	Digital In	Chip ID bit 3 (MSB).
96	DRE14_VCM_IN	Analog In	DRE external 600mV input.
97	DRE14_BLP_IN	Analog In	DRE external baseline input, positive.
98	DRE14_BLN_IN	Analog In	DRE external baseline input, negative.
99	VDDA_DRE	Power	1.2V analog VDD for DRE channels 1-4.
100	VDDA_DRE	Power	1.2V analog VDD for DRE channels 1-4.

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Table 1 – *Continued from previous page*

Pin	Name	Direction	Description
Pad	GND	Power	Ground. This must have a low-impedance connection to the circuit ground for good electrical performance and heat dissipation.

4 Electrical Interface

The COLUTAV3 device must be driven according to the specifications described within this section for optimal performance. All analog inputs are differential and are DC-coupled to the CMOS circuitry within the chip. Electrical interfacing to the COLUTAV3 analog inputs are summarized in table 2.

Temp=entire range, all corners, VDD=1.2V

Specification	**Notes**	**Min**	**Typ**	**Max**	**Units**
C_L Capacitive load	Single-ended value		8		pF
V_{FS} Full-scale swing	Differential			2.0	Volts pk-pk
$V_{FS[U,L]}$ Input range	Single-ended. With respect to ground.	0.1		1.1	Volts
V_{CM} Common-mode input voltage	VDD/2		0.6		Volts

Table 2: Requirements for driving the analog inputs.

5 I²C Control Format

The COLUTAV3 is intended to be used as an I²C slave device. The control structure of the chip features independently addressable write-only bits, where these bits are partitioned on a per-channel basis ("channel slow-control") and a set of general-purpose use bits ("global slow-control"). The on-chip I²C controller addresses uses one-hot encoding to address the slow-control blocks, thus all slow-control bits may either be addressed individually or simultaneously according to table 3. The global slow-control bank contains 24 read-only bits in addition to its write-only bits. The I²C slave controller can independently address up to eight channel slow-control blocks and the global slow-control block.

Address	Destination
8'h01	Channel 1 (DRE+SAR)
8'h02	Channel 2 (DRE+SAR)
8'h04	Channel 3 (DRE+SAR)
8'h08	Channel 4 (DRE+SAR)
8'h10	Channel 5 (MDAC+SAR)
8'h20	Channel 6 (MDAC+SAR)
8'h40	Channel 7 (MDAC+SAR)
8'h80	Channel 8 (MDAC+SAR)

Table 3: Channel slow-control addressing.

5.1 Channel Slow-Control Control Bits

Tables 4, 5, 6, 7, and 8 detail the assignments of the channel slow-control bits that are identical to every channel. Table 5 is only applicable to channels 1-4, while 6 is only applicable to channels 5-8 as they are mutually exclusive. The highest bit position indicates the most-significant bit.

Table 4: Channel-wide slow-control bit mapping.

sc_ch<>	Description
<543>	**CH:DATA_TX Drive Strength** Default: 1'b1
<542>	**CH:FRAME_TX Drive Strength** Default: 1'b1
<541>	**CH:DATA_MUX Select** Default: 1'b0 1'b0: Current channel data A 1'b1: Adjacent channel data B
<540:536>	**Un-used**
<535>	**CH:TP1 Pass-thru** Default: 1'b0
<534>	**CH:DISABLE** Default: 1'b0 1'b0: Channel analog biasing enabled. 1'b1: Channel analog biasing disabled.
<533:531>	**CH:Testpoint Select** Default: 3'h0 3'b000: TP1=GND; TP2=GND or MDAC_VREFN 3'b001: TP1=GND; TP2=GND 3'b010: TP1=VDD_DRE or VDD_MDAC; TP2=GND or MDAC_VCM 3'b011: TP1=GND; TP2=GND 3'b100: TP1=VDD_AMP_SAR; TP2=VDD_REF_SAR 3'b101: TP1=GND; TP2=GND 3'b110: TP1=TP1_thru; TP=TP2_thru 3'b111: TP1=25μA sink; TP2=GND
<530:529>	**Un-used**
<528>	**CH:TP2 Pass-thru** Default: 1'b1

Table 5: Channel DRE slow-control bit mapping. Applicable only to channels 1-4.

sc_ch<>	Description
<527:524>	**Un-used**
<523:518>	**DRE:REFDAC** Default: 6'h24
<517>	**DRE:CalOn** Default: 1'b0
<516>	**DRE:CalConfig1** Default: 1'b1
<515>	**DRE:MS** Default: 1'b0 1'b0: Auto-gain 1'b1: Manual select
<514>	**DRE:GS** Default: 1'b1 1'b0: 4x gain 1'b1: 1x gain
<513>	**DRE:EnKickbackShorter** Default: 1'b1
<512>	**DRE:OutExtEn** Default: 1'b0
<511:504>	**DRE:IDAC** Default: 8'hA8
<503>	**DRE:CLKEN** Default: 1'b1
<502':500>	**DRE:AmpSt2EN** Default: 3'h0
<499:496>	**DRE:MDAC_CAL** Default: 4'h8
<495:491>	**DRE:CAPGAIN** Default: 5'b0
<490>	**DRE:conVREF** Default: 1'b0
<489>	**DRE:BLShift_SA** Default: 1'b0
<488>	**DRE:BLEN_SUBADC** Default: 1'b0
<487:440>	**Un-used**

Table 6: Channel MDAC slow-control bit mapping. Applicable only to channels 5-8.

sc_ch<>	Description
<527:524>	**Un-used**
<523>	**MDAC:PAD_EN** Default: `1'b0` `1'b0`: Output to external pad disabled `1'b1`: Output to external pad enabled
<522>	**MDAC:CLK_EN** Default: `1'b1`
<521>	**MDAC:FLAG_EN** Default: `1'b1`
<520:516>	**MDAC:CAPGAIN** Default: `4'h0`
<515:508>	**MDAC:IDAC** Default: `8'hA8`
<507:505>	**MDAC:AMP_STG2** Default: `3'h2`
<504>	**MDAC:CAL_EN** Default: `1'b0`
<503:496>	**MDAC:CAL_FLASH** Default: `8'h00`
<495:488>	**MDAC:CAL_MDAC** Default: `8'h00`
<487>	**MDAC:CB_M_EN** Default: `1'b1`
<486:485>	**MDAC:CB_M_STGTWO** Default: `2'h1`
<484:479>	**MDAC:CB_M_IREF** Default: `6'h6B`
<478>	**MDAC:CB_M_ONCHIP** Default: `1'b1`
<477>	**MDAC:CB_C_EN** Default: `1'b1`
<476:475>	**MDAC:CB_C_STGTWO** Default: `2'h0`
<474:469>	**MDAC:CB_C_IREF** Default: `6'h29`
<468>	**MDAC:CB_C_ONCHIP** Default: `1'b1`
<467>	**MDAC:CB_P_EN** Default: `1'b1`

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Table 6 – *Continued from previous page*

sc_ch<>	Description
<466:465>	**MDAC:CB_P_STGTWO** Default: 2'h2
<464:459>	**MDAC:CB_C_IREF** Default: 6'h29
<458>	**MDAC:CB_C_ONCHIP** Default: 1'b1
<457:440>	**Un-used**

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Table 7: Channel SAR slow-control bit mapping.

sc<>	Description
<439>	**SAR:EN_RB_VREFN** Default: 1'b1
<438>	**SAR:EN_RB_VCM** Default: 1'b1
<437>	**SAR:EN_RB_VREFP** Default: 1'b1
<436>	**SAR:RB2EXT_VREFN_FStage** Default: 1'b0
<435>	**SAR:RB2EXT_VREFN_CStage** Default: 1'b0
<434>	**SAR:RB2EXT_VCM** Default: 1'b0
<433>	**SAR:RB2EXT_VREFP_FStage** Default: 1'b0
<432>	**SAR:RB2EXT_VREFP_CStage** Default: 1'b0
<431>	**SAR:SHORT_INPUT** Default: 1'b0
<430>	**SAR:DREMDAC_TO_SAR** Default: 1'b1
<429>	**SAR:EXT_TO_SAR** Default: 1'b0
<428>	**SAR:CLK_EN** Default: 1'b1
<427>	**SAR:S_AMP** Default: 1'b1 1'b0: 50% decision cycle 1'b1: 25% decision cycle
<426:419>	**SAR:VREF_PBOOST** Default: 8'h37
<418:411>	**SAR:VREF_NBOOST** Default: 8'h37
<410:403>	**SAR:VREF_MAIN** Default: 8'h37
<402:397>	**SAR:IBIAS_FLOOP** Default: 6'h0D
<396:391>	**SAR:IBIAS_CLOOP** Default: 6'h0D
<390:385>	**SAR:IBIAS_RBCM** Default: 6'h0D

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Table 7 – *Continued from previous page*

sc<>	Description
<384:379>	**SAR:IBIAS_RBP** Default: 6'h0D
<378:373>	**SAR:IBIAS_RBN** Default: 6'h0D
<372:367>	**SAR:IBIAS_PBOOST** Default: 6'h0D
<366:361>	**SAR:IBIAS_NBOOST** Default: 6'h0D
<360:355>	**SAR:IBIAS_MAIN_OP** Default: 6'h0D
<354:335>	**SAR:CAL_REGB** Default: 20'h00000
<334:315>	**SAR:CAL_REGA** Default: 20'h00000
<314>	**SAR:CAL_DIR** Default: 1'b0
<313>	**SAR:CAL_PN_DAC** Default: 1'b0
<312:291>	**SAR:CAL_EN** Default: 22'h000000

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Table 8: Channel DDPU slow-control bit mapping.

sc_ch<>	Description
<290:274>	**DDPU:MDAC Correction Code 7** Default: 17'b11100000000000000
<273:257>	**DDPU:MDAC Correction Code 6** Default: 17'b11000000000000000
<256:240>	**DDPU:MDAC Correction Code 5** Default: 17'b10100000000000000
<239:223>	**DDPU:MDAC Correction Code 4** Default: 17'b10000000000000000
<222:206>	**DDPU:MDAC Correction Code 3** Default: 17'b01100000000000000
<205:189>	**DDPU:MDAC Correction Code 2** Default: 17'b01000000000000000
<188:172>	**DDPU:MDAC Correction Code 1; DRE pedestal** Default: 17'b00100000000000000
<171:155>	**DDPU:MDAC Correction Code 0; DRE g1 offset** Default: 17'b00000000000000000
<154:141>	**DDPU:SAR Correction Code 20** Default: 14'b11100000000000
<140:127>	**DDPU:SAR Correction Code 19** Default: 14'b10000000000000
<126:114>	**DDPU:SAR Correction Code 18** Default: 13'b1000000000000
<113:102>	**DDPU:SAR Correction Code 17** Default: 12'b101000000000
<101:91>	**DDPU:SAR Correction Code 16** Default: 11'b11000000000
<90:80>	**DDPU:SAR Correction Code 15** Default: 11'b10000000000
<79:70>	**DDPU:SAR Correction Code 14** Default: 10'b1000000000
<69:60>	**DDPU:SAR Correction Code 13** Default: 10'b1110000000
<59:50>	**DDPU:SAR Correction Code 12** Default: 10'b1000000000
<49:41>	**DDPU:SAR Correction Code 11** Default: 9'b100000000
<40:33>	**DDPU:SAR Correction Code 10** Default: 8'b10000000
<32:26>	**DDPU:SAR Correction Code 9** Default: 7'b1100000

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Table 8 – *Continued from previous page*

sc_ch<>	Description
<25:19>	**DDPU:SAR Correction Code 8** Default: 7'b1000000
<18:13>	**DDPU:SAR Correction Code 7** Default: 6'b101000
<12:8>	**DDPU:SAR Correction Code 6** Default: 5'b11000
<7>	**DDPU:Serializer Test Mode** Default: 1'b0 1'b0: Normal data 1'b1: Test pattern
<6>	**DDPU:Correction Enable** Default: 1'b1
<5>	**DDPU:Output Mode** Default: 1'b0 1'b0: Normal 16-bit mode 1'b1: Debug 32-bit mode
<4>	**DDPU:Flavor** Default: 1'b0 1'b0: DRE mode 1'b1: MDAC mode
<3:0>	**DDPU:LPGBT Phase** Default: 4'h0

5.2 Global Slow-Control Bits

The global slow-control bits (table 9) are allocated to shared resources including the clock distribution, on-chip bandgap, and test structure blocks. There exists 24 read-only bits.

TODO: Document read-only bits.

Table 9: Global controll bit mapping.

sc_global<>	Description
<127>	**CLK:INV_640** Default: `1'b0` `1'b0`: Inverted polarity `1'b1`: Normal polarity
<126:124>	**CLK:DELAY_640** Default: `3'b000`
<123:121>	**BGP:TRIM_UP** Default: `3'b000`
<121:118>	**BGP:TRIM_DOWN** Default: `3'b000`
<117>	**BGP:EXT_START** Default: `1'b0` `1'b0`: Normal operation `1'b1`: External stimulus Avoid operating at `1'b1` for a prolonged period of time.
<116>	**BGP:SEL_IBIAS** Default: `1'b1` `1'b0`: IBIAS_EXT `1'b1`: BGP
<115>	**BGP:SEL_AMPSRC** Default: `1'b1` `1'b0`: RDAC `1'b1`: BGP
<114>	**BGP:SEL_VREFP** Default: `1'b1` `1'b0`: RDAC `1'b1`: BGP+AMP
<113>	**BGP:SEL_VREFN** Default: `1'b1` `1'b0`: RDAC `1'b1`: BGP
<112>	**BGP:EN_VREFP** Default: `1'b1` `1'b0`: High-Z `1'b1`: Enabled

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Table 9 – *Continued from previous page*

sc_global<>	Description
<111>	**BGP:EN_VREFN** Default: 1'b1 1'b0: High-Z 1'b1: Enabled
<110:105>	**BGP:RDAC_CODE_VREFP** Default: 6'b000101
<104:99>	**BGP:RDAC_CODE_VCM** Default: 6'b011010
<98:93>	**BGP:RDAC_CODE_VREFN** Default: 6'b111010
<92:87>	**BGP:FDBK_CODE_VREFN** Default: 6'b100001
<86>	**TS:DISABLE** Default: 1'b0
<85:83>	**TS:TP12_SEL** Default: 3'b000 3'b000: XS thru 3'b001: IOA Backend 3'b010: TP1=XS_VBOT; TP2=XS_CMP 3'b011: TP1=XS_VBOT; TP2=XS_SEU 3'b100: TP1=XS_VBOT; TP2=XS_LR 3'b101: TP1=XS_nRST; TP2=XS_GATE 3'b110: Channel TP 3'b111: Global TP
<82:80>	**TS:TP12_MUX** Default: 3'b000 3'b000: Ch1 or {TP1=GND; TP2=GND} 3'b001: Ch2 or {TP1=BGP_VCM; TP2=50μA sink} 3'b010: Ch3 or {TP1=GND; TP2=GND} 3'b011: Ch4 or {TP1=VDD_BGP; TP2=VDD_CLK} 3'b100: Ch5 or {TP1=GND; TP2=GND} 3'b101: Ch6 or {TP1=GND; TP2=VDDD_DDPU} 3'b110: Ch7 or {TP1=GND; TP2=GND} 3'b111: Ch8 or {TP1=GND; TP2=GND}
<79>	**TS:DOUT_SEL** Default: 1'b0 1'b0: XS Measurement 1'b1: Slow-ADC

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Table 9 – *Continued from previous page*

sc_global<>	Description
<78:76>	**TS:DI_SEL** Default: 3'b000 3'b000: TP1=PIO; TP2=PLOGIC 3'b001: TP1=PIO4W; TP2=PLOGIC4W 3'b010: TP1=NIO; TP2=NLOGIC 3'b011: TP1=NIO4W; TP2=NLOGIC4W 3'b1xx: Replica current mirrors
<75>	**TS:DI_PASS** Default: 1'b0 1'b0: DI output disabled 1'b1: DI output enabled
<74:67>	**TS:DI_LOGIC** Default: 8'h80
<66:59>	**TS:DI_IO** Default: 8'h80
<58>	**TS:IOA_SWIN** Default: 1'b0 1'b0: Front-end 1'b1: Back-end
<57>	**TS:IOA_FEUG** Default: 1'b0 1'b0: Non-unity gain 1'b1: Unity gain
<56:53>	**TS:IOA_FEG** Default: 4'h0
<52:49>	**TS:IOA_BEG** Default: 4'h0
<48>	**TS:IOA_BEENABLE** Default: 1'b1
<47>	**TS:IOA_FEENABLE** Default: 1'b1
<46:43>	**TS:IOA_CAP** Default: 4'h8
<42:39>	**TS:IOA_BIAS** Default: 4'h5
<38>	**TS:XS_nRST** Default: 1'b0 1'b0: Reset 1'b1: Armed
<37:32>	**TS:XS_VT** Default: 6'h20

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Table 9 – *Continued from previous page*

sc_global<>	Description
<31>	**TS:XS_VBOT_GND** Default: 1'b0 1'b0: High-Z 1'b1: Grounded
<30>	**TS:XS_THRU** Default: 1'b0 1'b0: High-Z 1'b1: Thru
<29:27>	**TS:XS_SEUSEL** Default: 3'b000 3'b000: Open 3'b001: Short 3'b010: APS1 3'b011: APS2 3'b100: MOM1 3'b101: MOM2 3'b110: MIM1 3'b111: MIM2
<26>	**TS:XS_RSTMODE** Default: 1'b1 1'b0: Auto 1'b1: RSTMAN
<25>	**TS:XS_RSTMAN** Default: 1'b0 1'b0: Open 1'b1: Closed (reset)
<24:19>	**TS:XS_LR_TAP2** Default: 6'h08
<18:13>	**TS:XS_LR_TAP1** Default: 6'h02
<12:11>	**TS:XS_LR_PS** Default: 2'b00 2'b00: 156.25 kHz 2'b01: 312.5 kHz 2'b10: 625 kHz 2'b11: 1.25 MHz
<10>	**TS:XS_LR_MODE** Default: 1'b0 1'b0: Internal 1'b1: Prescaler

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Table 9 – *Continued from previous page*

sc_global<>	Description
<9>	**TS:XS_GTMODE** Default: 1'b0 1'b0: Internal 1'b1: GTMAN
<8>	**TS:XS_GTMAN** Default: 1'b1 1'b0: Hold count 1'b1: Armed
<7:5>	**TS:XS_GTLEN** Default: 3'b000 3'b000: 0.8388 s 3'b001: 1.6777 s 3'b010: 3.3554 s 3'b011: 6.7109 s 3'b100: 13.4218 s 3'b101: 26.8435 s 3'b110: 53.6871 s 3'b111: 107.3742 s
<4>	**TS:XS_CMPPOL** Default: 1'b1 1'b0: VIN<VT 1'b1: VIN>VT
<3>	**TS:XS_AMPPOL** Default: 1'b0 1'b0: IOA_VOUTN 1'b1: IOA_VOUTP
<2>	**TS:MADC_nRST_GTMAN** Default: 1'b1 1'b0: Reset 1'b1: Active
<1:0>	**TS:MADC_CLKPS** Default: 2'b00 2'b00: divide-by-1 2'b01: divide-by-4 2'b10: divide-by-8 2'b11: divide-by-16

6 Data Output Format

The COLUTAV3 has an output bandwidth of ten 640Mbps serial lanes using sLVDS differential signaling voltage levels and are all intended for a direct and seamless electrical interface to the lpGBT [2]. In all cases, bits are ordered from <15> (MSB) to <0> (LSB).

6.1 FRAME Output

Both FRAME outputs on channels 1 and 8 are of fixed data structure with a data length of 16 bits (1 word). The bit ordering of the FRAME data output is shown in table 10. Two frame outputs exist in the case of data bifurcation to the lpGBT, therefore only sc_ch<542> control the TX drive strength of the respective FRAME output. Channels 2-7 sc_ch<542> are internally un-connected.

The FRAME signal is comprised of two pieces of information: **FRAME:FIRST** and **FRAME:BCNumber** and is reliant on the state of the bunch-crossing reset (BC reset) signal. BC reset is asserted by providing a differential logic 1 to the sLVDS inputs of BCR_P and BCR_N. It is de-asserted by providing a differential logic 0. During BC reset, **FRAME:FIRST** is asserted to 1'b1 and **FRAME:BCNumber** is 5'b00000. Once BC reset is de-asserted, **FRAME:FIRST** is de-asserted and **FRAME:BCNumber** increments by one. The counter counts upward every ADC sample and wraps around continuously, all the while **FRAME:FIRST** is kept to 1'b0 until BC reset is asserted again. The FRAME word and DATA words are aligned bit-wise and therefore the FRAME signal is used to modulo-32 timestamp each ADC sample in synchronization to BC reset.

Table 10: FRAME output bit mapping.

FRAME<>	**Description**
<15>	1'b1
<14>	1'b0
<13>	**FRAME:FIRST** 1'b0: Non-first sample 1'b1: BC Reset is asserted
<12:8>	**FRAME:BCNumber** Bunch-crossing counter
<7:0>	8'h00

6.2 Channel-to-DATA Mapping

The eight DATA outputs are individually configurable via slow-control between channel pairs (1,2), (3,4), (5,6), and (7,8). Three canonical arrangements of channel-to-data exist: normal, even calibration, and odd calibration. These are summarized in table 11. Calibration modes double the bandwidth per channel to allow for offline calibration of internal circuitry. Additionally, each DATA output has a test pattern that takes precedence to the channel data output and is asserted by setting sc_ch<7> of the respective channel. The test pattern bit ordering is shown in table 12. Bit

ordering of data word A for the MDAC DDPU flavor is shown in table 14. Bit ordering of data word A for the DRE DDPU flavor is shown in table 15. Bit ordering of data word B regardless of DDPU flavor is shown in table 16.

Output Mode	DATA1	DATA2	DATA3	DATA4	DATA5	DATA6	DATA7	DATA8
Normal	Ch. 1	Ch. 2	Ch. 3	Ch. 4	Ch. 5	Ch. 6	Ch. 7	Ch. 8
Even Calibration	Ch. 2B	Ch. 2A	Ch. 4B	Ch. 4A	Ch. 6B	Ch. 6A	Ch. 8B	Ch. 8A
Odd Calibration	Ch. 1A	Ch. 1B	Ch. 3A	Ch. 3B	Ch. 5A	Ch. 5B	Ch. 7A	Ch. 7B

Table 11: Data output modes.

Table 12: DATA output test pattern bit mapping.

DATA<>	Description
<15:12>	4'b1010
<11:8>	**DATA_SERTEST:CID** Same as Chip ID inputs from the pinout.
<7:5>	**DATA_SERTEST:CHN** Channel number in binary numbering from 3'b000 to 3'b111
<4:0>	5'b01001

6.3 Normal Data Mode

Normal data mode is a direct one-to-one assignment for each channel with a data length of 1 word per lane. The bit ordering of the normal data output per channel is shown in table 13. sc_ch<541> must be set to 1'b0 and sc_ch<5> must be set to 1'b0 for all eight channels. sc_ch<543> are equally mapped one-to-one to the DATA TX drive strength control of that output.

Table 13: DATA output bit mapping, normal mode.

DATA<>	Description
<15>	**DATA_NORM:OVERFLOW** 1'b0: ADC normal range 1'b1: ADC overflow
<14:0>	**DATA_NORM:ADC_COUNT** ADC binary output

6.4 Calibration Data Modes

In even calibration mode, even channels are brought out one-to-one while an auxiliary data stream takes the odd data outputs. sc_ch<541> must be set to 1'b0 for channels 2,4,6,8 and sc_ch<541> must be set to 1'b1 for channels 1,3,5,7. Meanwhile, sc_ch<5> must be set to 1'b1 for all channels. Note that sc_ch<543> is still a one-to-one mapping from channel slow-control to TX drive strength. Note that the appropriate DDPU flavor, sc_ch<4> must be set per channel.

In odd calibration mode, odd channels are brought out one-to-one while an auxiliary data stream takes the even data outputs. sc_ch<541> must be set to 1'b0 for channels 1,3,5,7 and sc_ch<541> must be set to 1'b1 for channels 2,4,6,8. Meanwhile, sc_ch<5> must be set to 1'b1 for all channels. Note that sc_ch<543> is still a one-to-one mapping from channel slow-control to TX drive strength. Note that the appropriate DDPU flavor, sc_ch<4> must be set per channel.

Table 14: DATA output bit mapping, calibration mode, MDAC flavor, word A.

DATA<>	**Description**
<15>	2'b00
<13>	**DATA_A_MDAC:BEFORE_EDGE** Only applicable to channel 8, otherwise 1'b0
<12>	**DATA_A_MDAC:AFTER_EDGE** Only applicable to channel 8, otherwise 1'b0
<11:4>	**DATA_A_MDAC:MDAC** MDAC raw bits Ch2: {{4'b1000}{**SLOWADC<11:8>**}} Ch4: **SLOWADC<7:0>**
<3:0>	**DATA_A_MDAC:SAR<19:16>** SAR raw data

Table 15: DATA output bit mapping, calibration mode, DRE flavor, word A.

DATA<>	Description
<15>	2'b00
<13>	**DATA_A_DRE:BEFORE_EDGE** Only applicable to channel 8, otherwise 1'b0
<12>	**DATA_A_DRE:AFTER_EDGE** Only applicable to channel 8, otherwise 1'b0
<11:7>	5'b00000
<6>	**DATA_A_DRE:C1** DRE C1
<5>	**DATA_A_DRE:C2** DRE C2
<4>	**DATA_A_DRE:GAIN** DRE Gain
<3:0>	**DATA_A_MDAC:SAR<19:16>** SAR raw data

Table 16: DATA output bit mapping, calibration mode, word B.

DATA<>	Description
<15:0>	**DATA_B:SAR<15:0>** SAR raw data

References

[1] ATLAS Collaboration, "Technical Design Report for the Phase-II Upgrade of the ATLAS LAr Calorimeter," CERN, Geneva, Tech. Rep. CERN-LHCC-2017-018. ATLAS-TDR-027, Sep 2017. [Online]. Available: https://cds.cern.ch/record/2285582

[2] "lpGBT," https://lpgbt.web.cern.ch/lpgbt/.